

Product brief

64-Mbit to 512-Mbit HYPERRAM™ 2.0/3.0 psuedostatic RAM memory

Overview

HYPERRAM™ is a high-speed, low-pin-count, low-power self-refresh Dynamic RAM (DRAM) for high-performance embedded systems requiring expansion memory for scratchpad or buffering purposes.

HYPERRAM products support JEDEC JESD251 profile compliant HYPERBUS™ and Octal xSPI interfaces that draw upon the legacy features of both parallel and serial interface memories, while enhancing system performance and ease of design, as well as reducing system cost. The low-pin count architecture make HYPERRAM especially suitable for power and board space constrained applications requiring off-chip external RAM.

Introduced in 2015, HYPERRAM now has a broad ecosystem support from leading MCU, MPU and FPGA chipset partners and customers. Optimized HYPERBUS™ memory controller is available from multiple third-party IP vendors.

Key Benefits

High Reliability

- > Support for extended industrial and automotive Grade 1 & 2 temperature ranges.
- > AEC-Q100-qualified parts and PPAP support available.

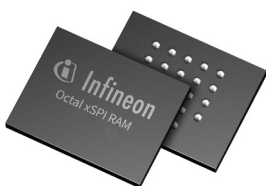
Target Applications

- > Automotive Instrument Clusters, Infotainment & Telematics Systems.
- > Industrial Machine Vision.
- > Industrial and Consumer HMI Display Panels.
- > Consumer Wearable Devices.
- > IoT Gateways and Communication Modules.

OCTAL xSPI RAM
64-Mbit to 512-Mbit |
400 MBps

HYPERRAM 2.0
64-Mbit to 512-Mbit |
400 MBps

HYPERRAM 3.0
256-Mbit | 800 MBps



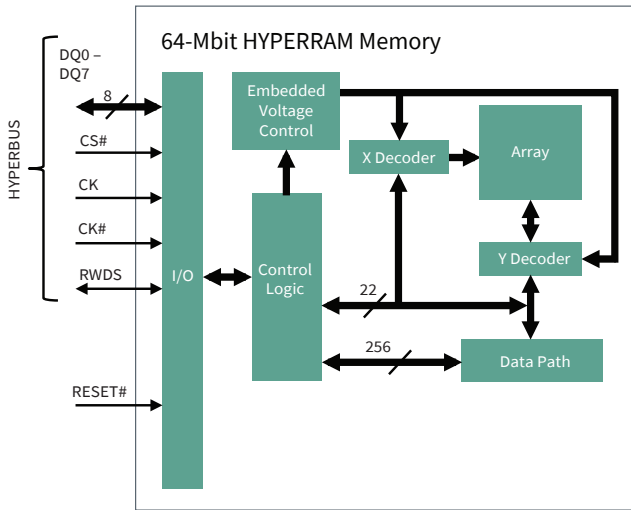
HYPERBUS interface

- > HYPERBUS is a high-bandwidth, 12 pin interface that transfers information at double data rate (DDR), delivering bandwidth of up to 400 MBps.
- > The HYPERBUS interface enables a small 48-mm² 24-ball package which shares a common footprint with HYPERFLASH™ products.
- > HYPERBUS is supported by a wide ecosystem of host controllers and memory types.

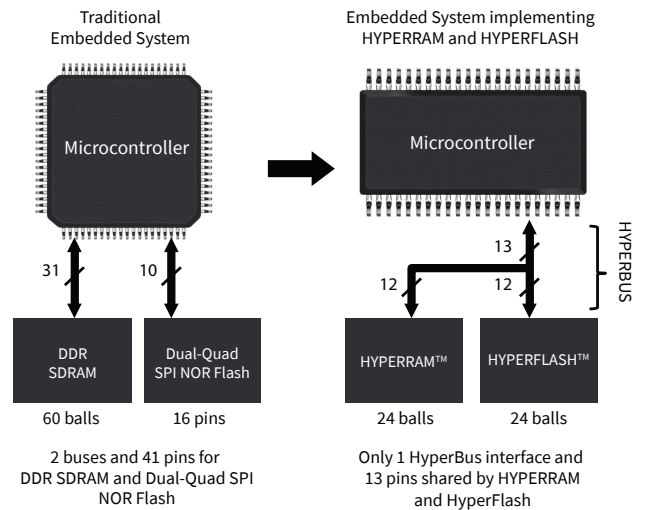
DRAM and FLASH on the same Bus

- > Reducing pin count simplifies design complexity and decreases system cost.
- > HYPERFLASH and HYPERRAM 2.0 can be placed on the same bus and only require 13 pins for data transactions (12-pin HYPERBUS + 1 additional chip-select for the second memory device).

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64-Mbit HYPERRAM Memory Block Diagram



Operating on a Single HYPERBUS Simplifies Designs and Reduces Pin Count

HYPERRAM 2.0 memory device portfolio

Family	Data-bus width	Interface	Speed	Voltage	Density	MPN	Bandwidth	Temperature range	Package
HYPERRAM 2.0	8-bit	HyperBus (x8)	200 MHz	1.8V	64-Mbit	S27KS0642	400 MBps	I, V, A, B, M	24-ball BGA (6 mm x 8 mm)
					128-Mbit	S70KS1282	400 MBps	I, V, A, B, M	
			256-Mbit	S80KS2562	400 MBps	I, V, A, B, M			
			512-Mbit	S80KS5122	400 MBps	I, V, A, B, M			
Octal xSPI RAM		Octal xSPI (x8)	200 MHz	1.8V	64-Mbit	S27KL0642	400 MBps, 333 MBps	I, V, A, B, M	
					128-Mbit	S70KL1282	400 MBps, 333 MBps	I, V, A, B, M	
			200 MHz, 166 MHz	3.0V	64-Mbit	S27KS0643	400 MBps	I, V, A, B	
					128-Mbit	S70KS1283	400 MBps	I, V, A, B	
HYPERRAM 3.0	16-bit	HyperBus Extended I/O (x16)	200 MHz	1.8V	256-Mbit	S80KS2564	800 MBps	I, V	49-ball BGA (8 mm x 8 mm)
					512-Mbit	S80KS5123	400 MBps	I, V, A, B, M	
			200 MHz, 166 MHz	3.0V	64-Mbit	S27KL0643	400 MBps, 333 MBps	I, V, A, B	
					128-Mbit	S70KL1283	400 MBps, 333 MBps	I, V, A, B	

To learn more about HYPERRAM™ Memory products, visit www.infineon.com/HYPERRAM

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