MT8390 IoT Application Processor Datasheet

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Document Revision History

Revision	Date	Description
1.0	2022-07-04	Official release
1.1	2022-09-26	• Modified Section 1.2 Ordering information • Modified DPTX and eDPTX speed from 8.1Gpbs to 5.4Gpbs • Modified Section 6.2 PLL Specification • Modified Figure 4-1 Ball map diagram • Modified Section 4.1.1 and 4.1.2 ball map tables • Modified Table 6-1 Maximum performance ratings
1.2	2022-11-16	• Modified Table 5-1 Absolute maximum ratings • Modified Table 5-3 Recommended operating conditions for power supply
1.3	2022-12-09	• Modified Section 4.4 Reserved and Unused Pin Handling Recommendations
1.4	2022-12-26	• Modified Figure 1-1 Functional block diagram • Modified Section 1.2 Ordering information • Modified Section 3.9.3.2 CSI Timing Characteristics • Modified Table 5-2 Storage condition • Modified Table 5-3 Recommended operating conditions for power supply
1.5	2023-02-16	• Replaced Table 5-16 CSI D-PHY TX electrical characteristics with CSI D-PHY RX electrical characteristics • Modified two typos in Table 3-34 CSI0 signal descriptions and Table 5-14 DSI D-PHY TX electrical characteristics

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1 Introduction

MT8390 is a highly integrated platform incorporating the following key features:

- Dual-core Arm® Cortex®-A78 processor
- Hexa-core Arm Cortex-A55 processor
- Arm Mali™-G57 MC3 3D Graphics Accelerator (GPU) with Vulkan® 1.1, OpenGL ES 3.2 and OpenCL™ 2.2
- Single-core AI Processor Unit (APU) Cadence® Tensilica®VP6 processor with AI Accelerator (AIA)
- Single-core Cadence HiFi 5 Audio Engine DSP
- LPDDR4(X): Up to 8 GB, with memory data rate up to LPDDR4(X)-3733
- DDR4: Up to 8 GB, with memory data rate up to DDR4-3200
- Display output supporting 4K30 + 4K60 resolution
- Image processing: 32MP @ 30fps for single camera capture; 16MP + 16MP @ 30fps for dual camera capture
- Video encoding: 4K @ 30 fps with HEVC/H.264
- Video decoding: 4K @ 75 fps with AV1/VP9/HEVC/H.264

Figure 1-1 shows the functional block diagram of the device.

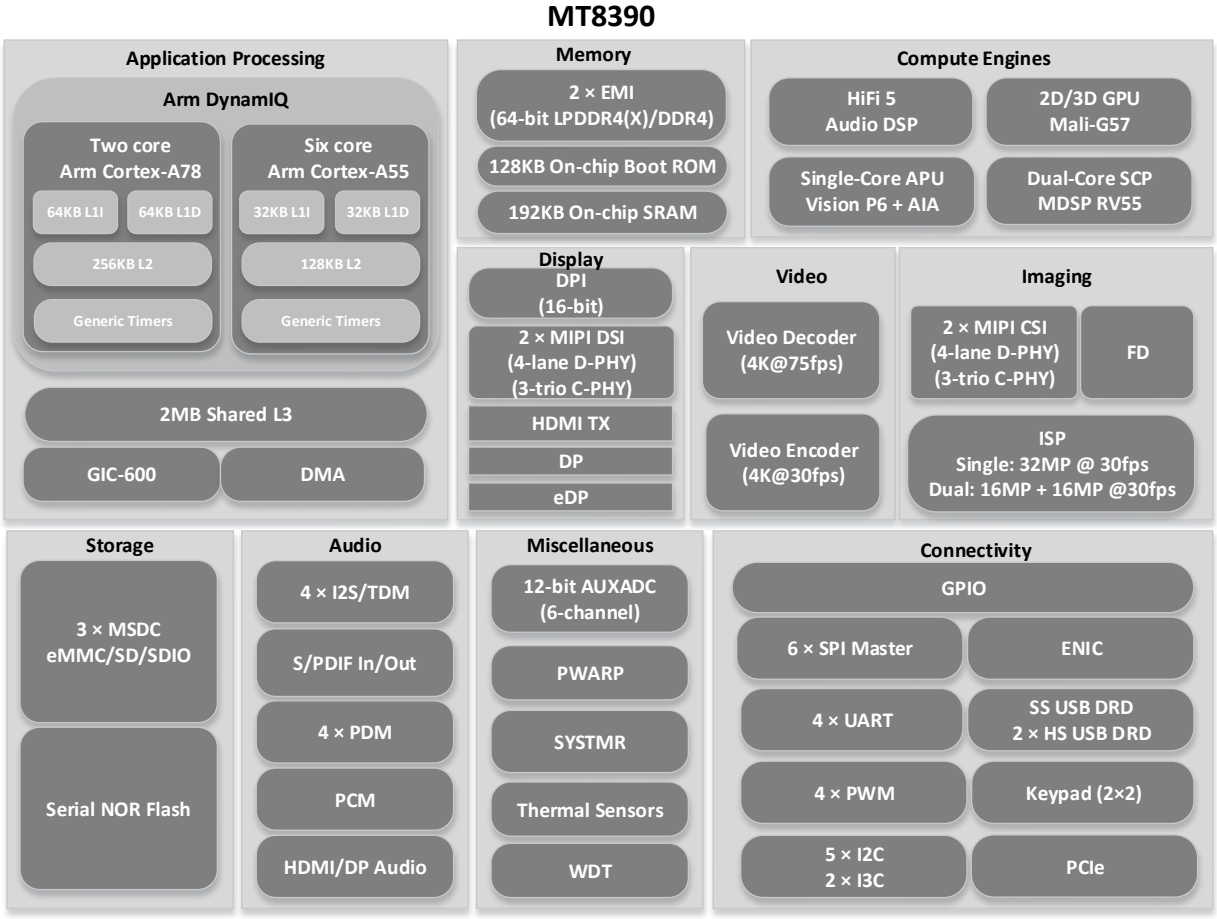

Figure 1-1 Functional block diagram

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1.1 Features Overview

Table 1-1 Device features

Feature		MT8390
Processors		
Dual-core Arm Cortex-A78	A78	2200 MHz
Hexa-core Arm Cortex-A55	A55	2000 MHz
Graphics Accelerator Mali-G57 MC3	GPU	950 MHz
HiFi 5 Digital Signal Processor	DSP	800 MHz
AI Processor Unit	APU	832 MHz
System Companion Processor	SCP	832 MHz
Memory		
External memory interface (LPDDR4(X)/DDR4)	EMI	Up to 8GB LPDDR4(X)-3733/DDR4-3200
Storage		
Memory Card Controller eMMC™/SD®/SDIO	MSDC0	eMMC (1-/4-/8-bit)
	MSDC1	SD/SDIO (1-/4-bit)
	MSDC2	SD/SDIO Card (1-/4-bit)
Serial NOR Flash Interface	SNOR	Yes
Display		
High-Definition Multimedia Interface Transmitter	HDMITX	HDMI™ 2.0b
Digital Display Parallel Interface	DPI	16-bit
DisplayPort Interface	DPTX	Yes (DP 1.4)
Embedded DisplayPort Interface	EDPTX	Yes (DP 1.2)
MIPI™ Display Serial Interface	DSI0	4-lane D-PHY, or 3-trio C-PHY
	DSI1	4-lane D-PHY, or 3-trio C-PHY
Imaging		
Image Signal Processor	ISP	Single camera: 32MP @ 30fps
		Dual camera: 16MP + 16MP @ 30fps
MIPI Camera Serial Interface 2	CSI0	1 × 4-lane D-PHY, or 2 × 2-lane D-PHY, or 1 × 3-trio C-PHY, or 2 × 2-trio C-PHY
	CSI1	1 × 4-lane D-PHY, or 1 × 3-trio C-PHY
Face Detection	FD	Yes
Warp Engine	WPE	Yes
JPEG Encoder	JPEG	Baseline encoding and decoding (250 MP/s)
Video		
Video Encoder	VENC	HEVC/H.264, 4K @ 30 fps
Video Decoder	VDEC	AV1/VP9/HEVC/H.264, 4K @ 75 fps
Audio		
Inter-IC Sound	I2S	4 (2 input, 2 output)
Time Division Multiplexed Interface	TDM	
Pulse Code Modulation	PCM	1
Pulse Density Modulation (Decoder for DMIC)	PDM	4 × stereo
Digital Interface	SPDIF_IN	2
	SPDIF_OUT	1

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Feature		MT8390
Inter-Integrated Circuit	I2C	5
	I3C	2[1]
Universal Asynchronous Receiver/Transmitter	UART	4
Serial Peripheral Interface	SPI	6 (master mode only)
Universal Serial Bus	USB Port 0	USB 2.0 DRD
	USB Port 1	SS USB 3.1 Gen1 DRD
	USB Port 2	USB 2.0 DRD
KeyPad Scanner	KeyPad	2 × 2
General Purpose I/O pins	GPIO	177
Pulse Width Modulation	PWM	Up to 4
Peripheral Component Interconnect Express	PCIe	Gen2, 1-lane, RC mode
Gigabit Ethernet Network Interface Controller	ENIC	MII/RMII/RGMII
Miscellaneous		
Auxiliary ADC	AUXADC	12-bit, 6-channel
Timers	GPT	5 × 32-bit and 1 × 64-bit
	SYSTMR	64-bit
	WDT[2]	Yes
Thermal Controller	TCSYS	Yes

1. I3C5 and I3C6 support MIPI I3C® (SDR mode only).
2. The Watchdog Timer (WDT) is part of the Top Reset Generation Unit (TOPRGU).

1.2 Ordering Information

Table 1-2 Ordering information

Order#	Marking	Temp. range	PCB thickness (T)	HDMI (RX/TX)	Package
MT8390AV/AZA	See Section 7.2 Top Marking	-20~65°C T_a	T ≤ 1.2mm	Yes	MFC-VFBGA

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2 Preface

2.1 Pin Characteristics and Signal Descriptions Conventions

Table 2-1 describes the column headers in all Pin Characteristic and Signal Description tables in Section 4.2 Pin Characteristics and Chapter 3 Features Description.

Table 2-1 Column headers description

Column name	Explanations
Ball Name	Logical name of the ball. Note that there may exist a selection of several signals for the same ball (aux mode).
Ball Location	Ball's physical location on the chip package
Signal Name	The name of the signal for the given aux mode
Type	Pin type when configured for the given aux mode: • AI: Analog input • AO: Analog output • AIO: Analog bi-directional pin • DI: Digital input • DO: Digital output • DIO: Digital bi-directional pin • P: Power • G: Ground
Description	Description of the signal
Aux. Function	Auxiliary function mode number: • 0 through 7 are possible alternative functions • An empty box means Not Applicable and the ball is dedicated to one function only
Reset State	Shows the Aux. function configured at the release of the SYSRSTB signal
Buffer Type	Describes the associated input/output buffer type
Power Domain	Indicates the voltage supply that powers the terminal IO buffers
PU/PD	Indicates the state of an internal pull-up or pull-down resistor at the release of the SYSRSTB signal: • OFF: Internal pull-up and pull-down are disabled • PU: Pull-up is enabled • PD: Pull-down is enabled • No: Pull-up and pull-down not available • Blank cell means "No"
IO Reset Value	Shows the IO state at the release of the SYSRSTB signal

2.2 Timing Conventions, Parameters, and Information

This section provides a general description of used symbols, adopted standards and terminology, and test process. All timing characteristics are valid over the represented operating conditions unless otherwise specified.
The interface clock frequency documented in this datasheet is the maximum clock frequency, which corresponds to the maximum programmable frequency on the particular output clock. The frequency defines the maximum limit supported by the device and does not consider into account any system limitation (layouts, connectors, and so forth).

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The system designer should take into account these system considerations and the device timing characteristics as well and should determine properly the maximum frequency supported to transfer the data on the corresponding interface. The timing parameter values do not include delays by board routes. Timing values may be adjusted by increasing/decreasing such delays. If needed, external logic hardware such as buffers may be used to compensate any timing differences.

2.2.1 Timing Parameters and Information

Table 2-2 represents timing parameter symbols and descriptions used in the timing characteristic tables.

Table 2-2 Timing parameters

Symbol	Description
f_{op}	Operating frequency
t_p	Period (cycle time)
t_d	Delay time
t_{dis}	Disable time
t_{en}	Enable time
t_h	Hold time
t_{su}	Setup time
Start	Start bit
t_t	Transition time
t_v	Valid time
t_w	Pulse duration
t_{FALL}	Fall time
t_{RISE}	Rise time
V_{OH}	High level output voltage
V_{OL}	Low level output voltage
V_{IH}	High level input voltage
V_{IL}	Low level input voltage
V_{REF}	Reference voltage

2.2.2 Parameter Information

This datasheet provides timing values at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be also taken into account.
All timing requirements and switching characteristics are valid over the recommended operating conditions unless otherwise specified.
All rise and fall transition timing parameters are referenced correspondingly to 90% and 10% of the signal logical levels, unless otherwise specified.

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2.3 Abbreviations

A

ADC
Analog to Digital Convertor
AER
Advanced Error Reporting
AES
Advanced Encryption Standard
AFBC
ARM Frame Buffer Compression
AHB
Advanced High-Performance Bus
AI
Artificial Intelligence
AIA
AI Accelerator
ALLM
Auto Low Latency Mode
APB
Advanced Peripheral Bus
APC
Address Protection Controller
APMCU
Application Processing Microcontroller Unit
APU
AI Processor Unit
ASP
Advanced Simple Profile
ASPM
Active State Power Management
ASRC
Asynchronous Sample Rate Converter
ASTC
Adaptive Scalable Texture Compression
AUXADC
Auxiliary Analog/Digital Converter
AV
Audio Video
AXI
Advanced eXtensible Interface

B

BBC
British Broadcasting Corporation

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C

CABC
Content Adaptive Backlight Control
CBS
Credit-based Shaper
CCC
Common Command Code
CDR
Clock and Data Recovery
CEC
Consumer Electronics Control
CG
Clock Gating
CKSQ
Clock Squarer
CMDQ
Command Queue
CRC
Cyclic Redundancy Check
CSC
Color Space Conversion
CSI
Camera Serial Interface
CTS
Clear to Send
CV
Computer Vision

D

DAA
Dynamic Address Assignment
DCM
Dynamic Clock Management
DDC
Display Data Channel
DDR
Dual Data Rate
DISP_AAL
Display Adaptive Ambient Light Controller
DISP_CCORR
Display Color Correction
DISP_MIXER
Display Mixer
DISP_MUTEX
Display MUTEX

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DISP_OVL

Display Overlay

DISP_POSTMASK

Display POSTMASK

DISP_PWM

Display Pulse Width Modulation

DMA

Direct Memory Access

DMIC

Digital Microphone

DP TX

DisplayPort Transmitter

DP TX AUX

DisplayPort Transmitter Auxiliary Channel

DPI

Display Parallel Interface

DRAM

Dynamic Random Access Memory

DRD

Dual-Role-Device

DRE

Dark Region Enhancement

DRM

Digital Rights Management

DSC

Display Stream Compression

DSD

Direct Stream Digital

DSI

Display Serial Interface

DSP

Digital Signal Processor

DVFS

Dynamic Voltage and Frequency Scaling

DVI

Digital Visual Interface

E

ECRC

Endpoint Cyclic Redundancy Check

EDID

Extended Display Identification Data

EEE

Energy Efficient Ethernet

EINT

External Interrupt

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EMI

External Memory Interface

ENIC

Ethernet Network Interface Controller

EOTF

Electro-Optical Transfer Function

F

FD

Face Detection

FIFO

First In First Out

FHD

Full High-Definition

FPU

Floating Point Unit

FSM

Finite State Machine

G

GIC

Generic Interrupt Controller

GPGPU

General Purpose computing on GPU

GPIO

General-purpose Input/Output

GPT

General-Purpose Timer

H

HDCP

High-bandwidth Digital Content Protection

HDMI

High Definition Multimedia Interface

HDMITX

High Definition Multimedia Interface Transmitter

HDR

High Dynamic Range

HEIF

High Efficiency Image File

HLG

Hybrid Log Gamma

HLOS

High-Level Operating System

HPD

Hot Plug Detect

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HSYNC
Horizontal Sync

I

I2C
Inter-Integrated Circuit
I2S
Inter-IC Sound
I3C
Improved Inter-Integrated Circuit
INTC
Internal Interrupt Controller
IoT
Internet of Things
IPC
Inter-Processor Communication
IRQ
Interrupt Request
ISP
Image Signal Processor

J

JTAG
Joint Test Action Group

L

L1PMSS
L1 Power Management Substates
L2TCM
L2 Tightly-Coupled-Memory
LFPS
Low Frequency Periodic Signaling
LPM
Lower power management
LSB
Least Significant Bit
LTR
Latency Tolerance Reporting
LUT
Look Up Table
LSP
Low Saturation Protection
LVTS
Low Voltage Thermal Sensor

M

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MAC
Medium Access Control
MBOX
Mailbox
MC
Motion Compensation
MCU
Microcontroller Unit
MDC
Management Data Clock
MDIO
Management Data Input/Output
MDLA
MediaTek Deep Learning Accelerators
MDP_AAL
Multimedia Data Path Adaptive Ambient Light Controller
MDP_FG
Multimedia Data Path Film Grain
MDP_TDSHP
Multimedia Data Path 2D Sharpness Engine
MDP_RDMA
Multimedia Data Path Read DMA
MDP_WROT
Multimedia Data Path Write Rotation
MDP_RSZ
Multimedia Data Path Resizer
MII
Media Independent Interface
MIPI
Mobile Industry Processor Interface
MISO
Master in slave out
MOSI
Master out slave in
MPU
Memory Protection Unit
MSB
Most Significant Bit
MSDC
MMC and SD Controller
MSI
Message Signaled Interrupt
MTL
MAC Transaction Layer
MUX
Multiplexer

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MV

Motion Vector

N

NN

Neural Network

NRZI

Non Return to Zero Invert

O

OETF

Optical-Electro Transfer Function

OSD

On-Screen Display

P

PBC

Peaking by Color

PCIe

Peripheral Component Interconnect Express

PCM

Pulse Code Modulation

PDM

Pulse Density Modulation

PHY

Physical Layer

PIO

Programmed Input/Output

PIPE

PHY Interface for PCI Express

PLL

Phase-Locked Loop

PMIC

Power Management Integrated Circuit

POR

Power-On-Reset

PPB

Private Peripheral Bus

PPS

Pulse-Per-Second

PWM

Pulse Width Modulation

PQ

Perceptual Quantizer

R

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RAS

Reliability, Availability and Serviceability

RC

Rate Control/Root Complex

RGMII

Reduced GMII

RH

Relative Humidity

RMII

Reduced MII

ROI

Region of Interest

RTC

Real Time Clock

RTOS

Real Time Operating System

RTS

Request to Send

RX

Receiver

S

SAR

Successive Approximation Register

SCLTM

Smart Contrast Local Tone Mapping

SCP

System Companion Processor

SDIO

Secure Digital Input/Output

SDM

Sigma-Delta Modulation

SDR

Single Data Rate/Standard Dynamic Range

SFD

Start of Frame Delimiter

SIMD

Single Instruction Multiple Data

SMI

Smart Multimedia Interface

SP

Strict Priority

SPDIF

Sony/Philips Digital Interface Format

SPI

Serial Peripheral Interface

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SPM

System Power Management

SRAM

Static Random Access Memory

SRC

Sampling Rate Converter

SSC

Spread Spectrum Clocking

SSUSB

SuperSpeed Universal Serial Bus

SW

Software

SYSRAM

System Static Random Access Memory

T

TCM

Tightly Coupled Memory

TDM

Time Division Multiplexing

TDMS

Transition-Minimized Differential Signaling

TE

Tearing Effect

TOPRGU

Top Reset Generation Unit

TSMCU

Thermal Sensing Micro Circuit Unit

TSN

Time-Sensitive Networking

TX

Transmitter

U

UART

Universal Asynchronous Receiver/Transmitter

UFO

Universal Frame Buffer Compression

UHD

Ultra High Definition

UI

Unit Interval

USB

Universal Serial Bus

UTM

USB2.0 Transceiver Macrocell

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V

VC
Virtual Channel
VENC
Video Encoder
VDEC
Video Decoder
VFPU
Vector Floating-Point Unit
VLD
Variable Length Decoding
VLIW
Very Long Instruction Word
VPP
Video Processing Pipe
VRR
Variable Refresh Rate
VSYNC
Vertical Synchronization

W

WDT
Watchdog Timer
WPE
Warp Engine
WRR
Weighted Round Robin

X

xHCI
Extensible Host Controller Interface

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3 Features Description

The MT8390 device is a highly-integrated, powerful platform designed for a wide range of Artificial Intelligence (AI) and Internet of Things (IoT) use cases requiring high-performance edge processing, advanced multimedia and connectivity capabilities, multiple high-resolution cameras, connected touchscreen displays, and use of a multi-tasking High-Level Operating System (HLOS).

The highly-capable octa-core application processor utilizes the Arm® DynamIQ™ technology by combining high-performance Cortex-A78 and power-efficient Cortex-A55 cores, equipped with Arm Neon™ engine. The application processor offers the necessary processing power to support the latest OpenOS, along with its demanding applications such as web browsing, email and games. This content can be enhanced by the 2D/3D graphics accelerator (Arm Mali-G57 MC3 GPU) and then visualized on a high-resolution touchscreen display. To provide advanced multimedia applications and services such as streaming audio and video, the device features multi-standard video encoder and decoder engines, and an advanced audio subsystem.

The AI Processor Unit (APU) enables deep learning, Neural Network (NN) acceleration, and Computer Vision (CV) applications. The latter, combined with the up to 32MP camera, can clearly and accurately perform AI-vision functions such as facial recognition, object identification, scene analysis, optical character recognition and much more.

An extensive set of interfaces, connectivity, flexible storage and memory options further enhance the capabilities of the device and give product designers freedom to customize.

3.1 Application Processors

The device includes an Arm processor based subsystem (MCUSYS), which is responsible for running operating system and application programs in the device. It comprises two different Arm CPUs: six Cortex-A55 (little) cores and two Cortex-78 (big) cores, residing into a single cluster (Arm DynamIQ). This implementation provides different levels of power efficiency and computing power to satisfy a wide range of system power and performance requirements. The power efficiency of the six little cores (A55) is specially optimized to minimize the power consumption in daily usage scenarios and lightweight applications. For performance driven applications, the two powerful big cores (A78) can handle the heavy tasks and provide the best user experience under these scenarios.

The DynamIQ cluster also includes:

- Arm DynamIQ Shared Unit
- 2M shared L3 cache for all CPU cores within the cluster

The MCUSYS includes Arm GIC-600 interrupt controller that provides interrupt support.

The MCUSYS supports Dynamic Voltage and Frequency Scaling (DVFS) technology allowing CPU cores to run at different frequency and voltage configurations for different application requirements. Besides DVFS, the power of each CPU can be turned off individually when not used. In standby mode, the MCUSYS can be completely shut down to further save power consumption and optimize the battery usage on mobile devices.

3.1.1 Cortex-A78 Processor

The A78 processor (Arm Cortex-A78 MPCore) supports the following key features:

- Two-core implementation (*big cores*)

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- Neon processing engine with SIMDv2/VFPv4 ISA
- Full compliance with ARMv8-A architecture:
  - AArch32 and AArch64 execution states at all Exception Levels (EL0 to EL3)
  - A64 instruction set
  - A32 instruction set (Arm instruction set in pre-Armv8 architectures)
  - T32 instruction set (Arm Thumb® instruction set in pre-Armv8 architectures)
- Support for various Arm extensions:
  - Armv8.1 extensions
  - Armv8.2 extensions
  - Armv8.3 (LDAPR instructions only)
  - Cryptography extensions
  - Reliability, Availability and Serviceability (RAS) extensions
- ARM Jazelle® technology
- In-order pipeline with direct and indirect branch prediction
- Generic timers supporting 64-bit count input from SYSTMR
- Level 1 (L1) and Level 2 (L2) cache memory with cache line length of 64 bytes:
  - 64KB L1 instruction cache (I-cache), L1I
  - 64KB L1 data cache (D-cache), L1D
  - 256KB private (not shared) L2 cache for each core
- Security
  - Arm TrustZone®

3.1.2 Cortex-A55 Processor

The A55 processor (Arm Cortex-A55 MPCore) supports the following key features:

- Six-core implementation (*little* cores)
- Neon processing engine with SIMDv2/VFPv4 ISA
- Full compliance with ARMv8-A architecture:
  - AArch32 and AArch64 execution states at all Exception Levels
  - A64 instruction set
  - A32 instruction set
  - T32 instruction set
- Support for various Arm extensions:
  - Armv8.1 extensions
  - Armv8.2 extensions
  - Armv8.3 (LDAPR instructions only)
  - Cryptography extensions
  - RAS extensions
- ARM Jazelle technology
- In-order pipeline with direct and indirect branch prediction
- Generic timers supporting 64-bit count input from SYSTMR
- L1 and L2 cache memory with cache line length of 64 bytes:
  - 32KB L1 instruction cache (I-cache), L1I
  - 32KB L1 data cache (D-cache), L1D
  - 128KB private (not shared) L2 cache for each core

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- Security
  - Arm TrustZone

3.2 Graphics Accelerator

The device graphics accelerator (GPU) is based on Arm Mali-G57 MC3 core. It is used to process extremely complicated graphics and perform general processing tasks assigned by the main application processor.

The GPU supports the following key features:

- An enhanced API feature set with high-performance support for both shader-based and fixed-function graphics APIs The supported graphics and compute API industry standards are:
  - OpenGL ES 1.1, 2.0, and 3.2
  - Vulkan 1.0 and 1.1
  - OpenCL 1.0, 1.1, 1.2, 2.0, 2.1, 2.2
- Anti-aliasing capabilities
- An effective core for General Purpose computing on GPU (GPGPU) applications
- High memory bandwidth and low power consumption for 3D graphics content
- Arm Frame Buffer Compression (AFBC) 1.3
- Adaptive Scalable Texture Compression (ASTC)
- 8-bit, 10-bit and 16-bit YUV input and output formats
- Secure processing of Digital Rights Management (DRM) protected content
- Bus protocol:
  - 1 × 256-bit Arm AMBA® 1 AXI master interface for external memory access
  - 1 × 32-bit Arm AMBA 1 AXI slave interface for GPU configuration
- L2 cache
  - 1 bank × 512KB
  - 4-way, set associative
- Cache coherency support:
  - Within GPU

3.3 Digital Signal Processor

The HiFi 5 Audio Engine Digital Signal Processor (DSP) is a highly optimized audio processor designed for efficient execution of audio and voice codecs and pre-/post-processing modules. It is a Single Instruction Multiple Data (SIMD) processor with ability to work in parallel on four 32-bit data items or eight 16-bit data items. The Very Long Instruction Word (VLIW) architecture supports the execution of up to five operations in parallel.

The HiFi 5 DSP supports the following key features:

- Single-core implementation
- CPU architecture:
  - Thirty-two 64-bit DR Registers
  - Eight 32 × 32-bit Multiply-Accumulate operations (MACs) per cycle
  - Sixteen 32 × 16-bit MACs, sixteen 16 × 16-bit and 8 x 8 MACs per cycle
  - Source compatible with HiFi 4
  - Five VLIW slots
  - Ability to issue two 128-bit loads, or one load and one store of 128-bit per cycle

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  - Eight single precision IEEE-754 floating-point MACs per cycle for enhanced audio and voice processing. Pair of 4-way SIMD units.
  - Special instructions to accelerate FFT
  - Sixteen half-precision IEEE-754 floating point MACs per cycle for accelerating floating-point speech networks. Pair of 8-way SIMD units.
  - Instructions to accelerate convolution and matrix multiplication
  - Neural Network Extension
  - Up to thirty-two 8 × 16, 4 × 16 and 8 × 8-bit MACs per cycle for supporting speech recognition
  - Extends the HiFi 5 DSP's capability with specialized instructions targeted for matrix vector multiplication
  - SIMD Single precision Vector Floating Point (SP-vFPU)
  - SIMD Half precision Vector Floating Point (HP-vFPU)
  - Fixed Point (16, 32-bit)
  - Dual Load/Store Unit
- Up to 3 timers
- Memory system:
  - Level 1: 64KB L1 I-cache + 128KB L1 D-cache
  - Level 2: 512KB L2 SRAM—Tightly Coupled Memory (TCM)
  - 128-bit system bus interface
- No data retention support for pre-fetch buffer, I-cache, D-cache, ITag, and Dtag
- Support for 25 interrupts
- Supports System Power Management (SPM) to control power sequence
- Dedicated UART (DSP_UART)
- Clock speeds:
  - 800 MHz at 0.75V

3.4 AI Processing Unit

The AI Processor Unit System (APU) is a high-efficient computing unit that is best suited for Neural Network (NN) and Computer Vision (CV) algorithms.

The APUSYS supports the following key features:

Programmable Vision Processor Unit (VP6) for both AI and CV

- 1 × APU implementation
  - Cadence VP6
  - L1 instruction memory: 64 KB RAM + 128 KB cache
  - L1 data memory: 128 KB RAM + 128 KB cache
  - Vector Floating-Point Unit (VFPU) to support high precision requirement applications
- TOPS performance:
  - Fix 8: 0.43 TOPS
  - Fix 16: 0.11 TOPS
  - FP16: 0.06 TOPS
  - FP32: 0.03 TOPS

AIA (or MDLA– MediaTek Deep Learning Accelerator) for high computation demanding Neural Network (NN) applications

- 1 × AIA implementation, to provide more TOPS

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- 512KB local memory (L1 memory) per core
- TOPS performance
  - Fix 8 × Fix 8: 3.7 TOPS
  - Fix 16 × Fix 8: 1.9 TOPS
  - Fix 16 × Fix 16: 0.9 TOPS
  - FP 16/BF 16: 0.9 TOPS
- Simultaneous pipelined HW function block (CONV/ACT/POOL/EWE/BILINEAR)
- Sparsity-aware convolutions to skip redundant MAC cycles
- Enhancement of layer fusion to further reduce DRAM/TCM memory bandwidth
- Support for Android NN asymmetric quantized data format
- Support for compressed activation & weight to reduce DRAM BW

APUSYS memory subsystem

- eDMA engine for reduced-overhead data movement and format conversion

3.5 System Companion Processor (SCP)

System Companion Processor (SCP) is a micro-processor sub-system that includes two MDSP RV55 processors and a variety of peripherals. The special design of the SCP makes it suitable for running applications such as Voice wake-up, Sensor HUB and future tasks.

3.5.1 MDSP RV55 Features

The MDSP RV55 is a low-power DSP for sensor/voice/audio applications.

It supports the following key features:

- 32-bit integer core
- Single-precision Floating-Point Unit (FPU)
- Memory protection unit
- RISC-V compatible instruction set
- 6-stage pipeline, IF/PD/ID/E1/E2/WB
- L1 cache memory system:
  - 32KB I-cache
  - 32KB D-cache
- AXI interface and prefetch

Table 3-1 MCUSYS function block list

Name	MCU	L2TCM	SYSRAM	ROM	Other features
SCP subsystem	RV55x2 @832MHz	Total 1MB L2TCM	No	No	MPU, SWD, FPU

3.5.2 SCP Features

The SCP supports the following key features:

- Built-in 1 MB L2 Tightly-Coupled-Memory (L2TCM)
- Instruction memory and data memory share the 1MB TCM.
- An AXI Master interface to access L2TCM and Bus Fabric
- An AXI Master interface to access SoC-site INFRA and DRAM

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- An AXI Master interface to access ADSP shared L2TCM
- An AXI Slave interface for APMCU to access the SCP peripherals and configuration registers
- Six 32-bit down-count timers per core, with selectable clock source
- Internal Interrupt Controller (INTC) provides interrupt mask, interrupt group and asynchronous clock domain protection for accessing RV55 VIC.
- External Interrupt Controller (EINT) provides de-bounce (anti-glitch) and edge detection function for integrating external interrupt signals.
- 1 × I2C
- 1 × I3C
- 3 × SPI-M (masters)
- 2 × UART
- 2 × DMAs, which consist of 4-channel full-size DMA
- 8 GPIO pins
- Direct path to PMIC wrapper
- Watchdog Timer (WDT)
- Mailbox (MBOX) and Inter-Processor Communication (IPC) support for communication between SCP and APMCU

3.5.3 SCP Signal Descriptions

Table 3-2 presents SCP signal descriptions.

Table 3-2 SCP signal descriptions

Signal name	Type	Description	Ball location
SCP_ I3C0			
SCP_SCL0	DIO	SCP I3C clock 0	Y4, Y2, W2, F5, H7, T9
SCP_SDA0	DIO	SCP I3C data 0	W6, AA2, W1, F6, G6, T10
SCP_I2C0			
SCP_SCL1	DIO	SCP I2C clock 0	Y2, W2, F5, H7, T8, Y4
SCP_SDA1	DIO	SCP I2C data 0	AA2, W1, F6, G6, T7, W6
SCP_SPI0			
SCP_SPI0_CK	DO	SCP SPI0 serial clock	T11
SCP_SPI0_CS	DO	SCP SPI0 chip select	V6
SCP_SPI0_MI	DI	SCP SPI0 master input / slave output	V8
SCP_SPI0_MO	DO	SCP SPI0 master output / slave input	V7
SCP_SPI1_A			
SCP_SPI1_A_CK	DO	SCP SPI1 serial clock	T10
SCP_SPI1_A_CS	DO	SCP SPI1 chip select	T9
SCP_SPI1_A_MI	DI	SCP SPI1 master input / slave output	T7
SCP_SPI1_A_MO	DO	SCP SPI1 master output / slave input	T8
SCP_SPI1_B			
SCP_SPI1_B_CK	DO	SCP SPI1 serial clock	AC31
SCP_SPI1_B_CS	DO	SCP SPI1 chip select	AD30
SCP_SPI1_B_MI	DI	SCP SPI1 master input / slave output	AB31
SCP_SPI1_B_MO	DO	SCP SPI1 master output / slave input	AC30
SCP_SPI2			
SCP_SPI2_CK	DO	SCP SPI2 serial clock	G1

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Signal name	Type	Description	Ball location
SCP_SPI2_CS	DO	SCP SPI2 chip select	G2
SCP_SPI2_MI	DI	SCP SPI2 master input / slave output	E2
SCP_SPI2_MO	DO	SCP SPI2 master output / slave input	F2
SCP_UART			
TP_UCTS1_AO	DI	SCP UART1 clear to send (active low)	G5, U5
TP_UCTS2_AO	DI	SCP UART2 clear to send (active low)	E2, AB31, AA5
TP_URTS1_AO	DO	SCP UART1 request to send (active low)	E3, U4
TP_URTS2_AO	DO	SCP UART2 request to send (active low)	F2, AC5, AC30
TP_URXD1_AO	DI	SCP UART1 receive data	G3, U3, V2
TP_URXD2_AO	DI	SCP UART2 receive data	U3, AC31, U5, G1, AB5
TP_UTXD1_AO	DO	SCP UART1 transmit data	G4, U2, V1
TP_UTXD2_AO	DO	SCP UART2 transmit data	U2, AD30, U4, G2, AB6
SCP_GPIO			
TP_GPIO0_AO	DIO	SCP GPIO0	Y10, W5, AB32, AB9
TP_GPIO1_AO	DIO	SCP GPIO1	U10, V4, AA35, AC9
TP_GPIO2_AO	DIO	SCP GPIO2	Y6, V5, G4, AB8
TP_GPIO3_AO	DIO	SCP GPIO3	Y7, W8, G3, AC4
TP_GPIO4_AO	DIO	SCP GPIO4	Y8, R31, E3, R34, AB3
TP_GPIO5_AO	DIO	SCP GPIO5	W7, T30, G5, R33, AA8
TP_GPIO6_AO	DIO	SCP GPIO6	W3, T31, E4, T33, AC8
TP_GPIO7_AO	DIO	SCP GPIO7	W4, U32, E5, P31, AB7
SCP Command Signals			
SCP_VREQ_VAO	DO	SCP to PMIC normal voltage request	M31
Voice Wake-up			
VOW_CLK_MISO	DI	Voice wake-up interface clock	M32
VOW_DAT_MISO	DI	Voice wake-up interface data	M30

3.5.4 Block Diagram

Figure 3-1 shows the detailed block diagram of SCP sub-system as well as the connection interfaces with other modules (e.g. APMCU) or external IO pins. Some SCP major features are shown as below:

- Direct Memory Access (DMA)
  - DMA is useful when CPU (RV55 or APMCU) cannot keep up with the rate of data transfer, or when CPU needs to perform work while waiting for a relatively slow I/O data transfer.
  - For memory-to-memory (e.g. L2TCM ↔ L2TCM) data moving or memory-to-peripheral (e.g.L2 TCM ↔ I2C/I3C) data transmissions.
- L2TCM
  - The total size of L2TCM is 1MB. The program code and data for SCP are downloaded to L2TCM and the code is fetched directly from this memory space.
  - It stores the data received from serial communication interface (e.g. I2C, I3C, UART, SPI and GPIO) and loads the data transmitted to the serial communication interface. Therefore, APMCU or RV55 can require the data by accessing this memory space.
- Interrupt Controller (INTC and EINT)

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  - The INTC module is used to pre-integrate all interrupt sources into RV55 VIC, providing mask/unmask control and polarity configuration for each interrupt signal. It can also group the similar interrupt together.
  - The EINT module is used for de-bounce (anti-glitch) and edge detection function to stabilize the external IO interrupt source, which is located ahead of INTC.
- Serial Communication interfaces (e.g. I2C, I3C, SPI-M, UART, GPIO)
  - Several kinds of serial communication interfaces and general purpose I/O are provided to connect with external devices or to printout some information logs.
- SCP mailbox (SCP < - > APMCU)
  - There are virtual addresses allocated to L2TCM physical address function in SCP mailbox. Therefore, the APMCU can write down the message to inform each other that the programmable task has been completed or has exchanged data.
  - While the message is presented in L2TCM, users can write the command into mailbox command register. This mechanism will trigger an interrupt to inform APMCU or RV55 that there are messages presented in corresponding L2TCM (physical address).
- Clock Controller
  - The controller includes clock source MUX, clock divider and clock gate. According to the DVFS table and current application scenario, it can be programmable to generate the SCP internal clocks.
- Timer/Watchdog Timer (WDT)
  - Timer is a counter whose time intervals are programmable. Users can set the counter's initial value and enable the timer. When the timer counts down to zero, it will trigger a timeout interrupt to inform RV55.
  - A watchdog timer is an electronic timer that is used to detect RV55 malfunctions. During the normal operation, the RV55 regularly resets the watchdog timer to prevent it from "timing out". If, due to a hardware fault or a program error, the computer fails to reset the watchdog, the timer will elapse and generate a timeout interrupt to inform APMCU that RV55 stop working.

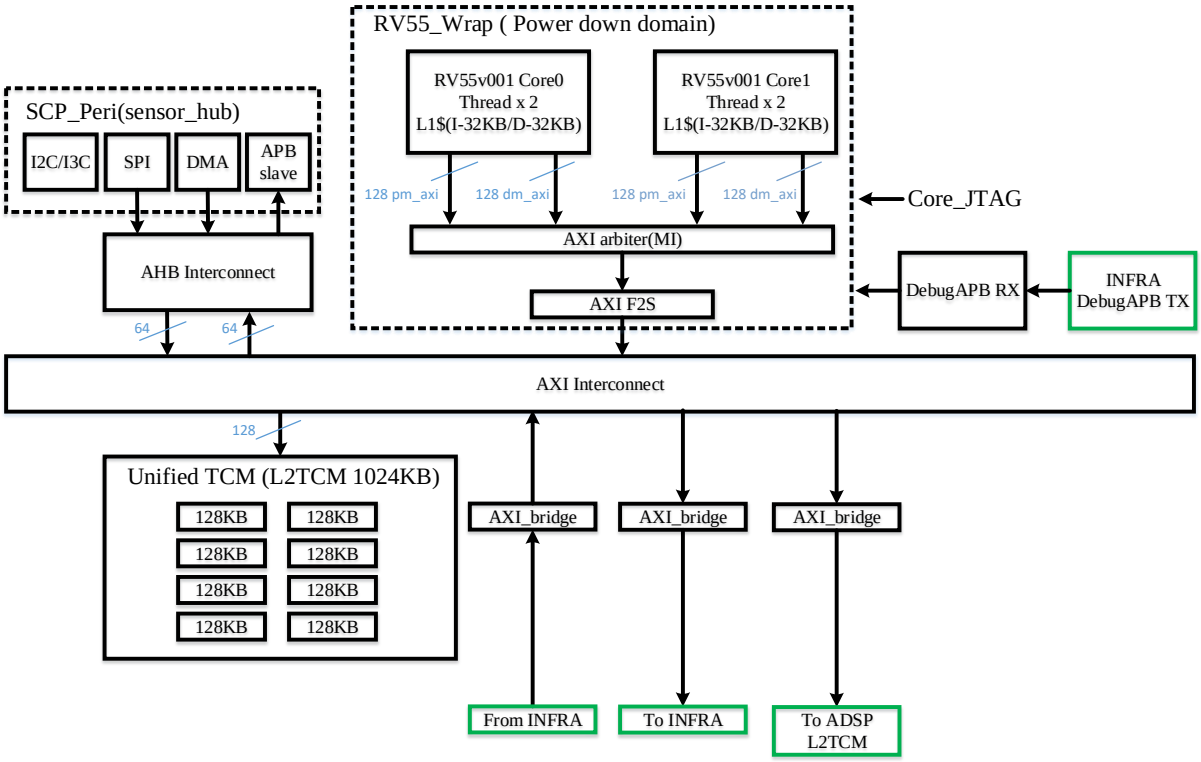

Figure 3-1 SCP Sub-system block diagram

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3.5.5 Clock Generation

3.5.5.1 Clock Structure for RV55 and Bus

The clock source of the SCP sub-system is provided by HF_FSCP_CK, CLK_32K, CLK_26M or CLK_ULPOSC (the four clocks are configured by the CLK_SW_SEL control register CR setting. Bus, RV55 and IP bus interface clock are controlled by the divider selection (MUX) control register and Clock Gating (CG) control register. The SCP clock structure is shown in Figure 3-2.

Note: When switching clock source, please guarantee that the destination clock source exists.

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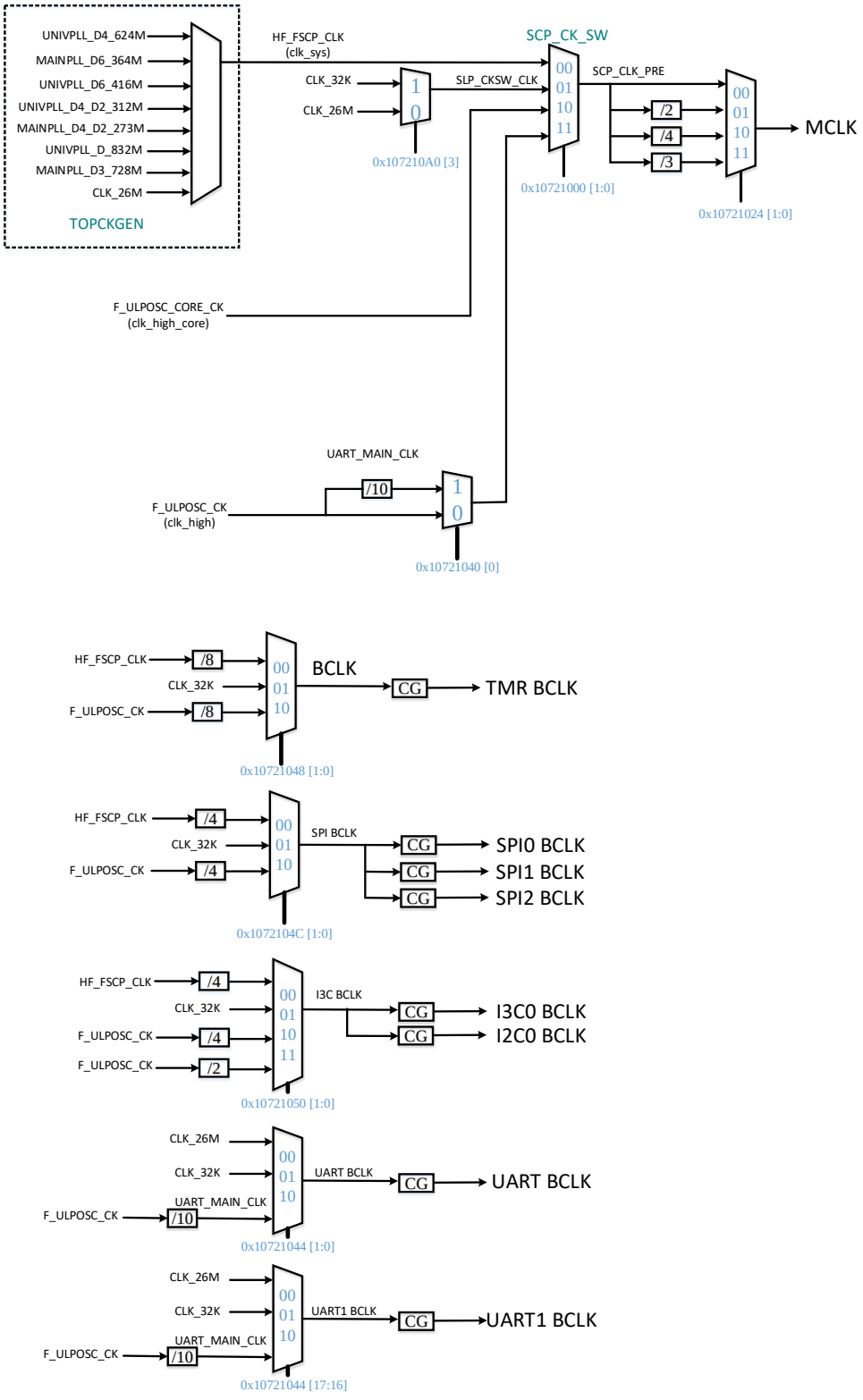

Figure 3-2 SCP clock structure

The SCP clock control is also responsible for SCP sleep control. When RV55 enters the idle state (waiting for interrupt), the clock controller will automatically change the SCP system clock to the slow clock of 32 kHz or 26 MHz. The SCP system will be resumed (clock is resumed to the fast clock) after the IRQ triggers the INTC which will be introduced in Section 3.5.8.

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3.5.5.2 Clock Structure for Low-Speed Peripherals and IO

In order to comply with the low-speed IO protocol, the peripherals need to operate at the special clock period (I2C bclk, I3C bclk, SPI bclk, UART bclk). The clock divider selection control register and the Clock Gating (CG) control register of low-speed peripherals and IO are shown in Figure 3-2.

3.5.5.3 Clock Structure Programming Outline

Table 3-3 Clock selection programming outline

Step	Sequence	REG_Name	REG_Value	Address
1	Select SCP system clock source	CLK_SW_SEL	User defined	SCP/AP Base Address + 0x21000
2	Select SCP system clock divider	CLK_DIV_SEL	User defined	SCP/AP Base Address + 0x21024
3	Enable SCP system clock gating (default off)	CLK_CG_CTRL	User defined	SCP/AP Base Address + 0x21030
4	Select peripherals clock source	I2C_BCLK_CK_SEL SPI_BCLK_CK_SEL UART_BCLK_CK_SEL I3C_BCLK_CK_SEL TMR_BCLK_CK_SEL	User defined	SCP/AP Base Address + 0x21050(I2C) SCP/AP Base Address + 0x2104C(SPI) SCP/AP Base Address + 0x21044(UART) SCP/AP Base Address + 0x21050(I3C) SCP/AP Base Address + 0x21048(TMR)
5	Enable peripherals clock gating (default off)	CLK_CG_CTRL	User defined	SCP/AP Base Address + 0x21030

3.5.6 JTAG

SCP RV55 supports two kinds of interfaces for CM4 debug: one is the dedicated JTAG from Pinmux; and the other is from APMCU debug top DAP interface.

3.5.7 Internal Bus Fabric

SCP bus fabric provides interconnection between IP cores. This interconnected system consists of AXI bus fabric, AHB bus fabric and APB bus fabric, which are shown in Figure 3-1. The AXI bus supports AXI master (RV55 and APMCU), and the AHB bus supports AHB master (DMA, SPI-M) and AHB slave (APB bus fabric) for high bandwidth data transfer. However, for low power application, the peripheral and SCP control register are connected to APB bus fabric.

3.5.8 Interrupt Controller

3.5.8.1 Internal Interrupt Controller (INTC)

The Interrupt Controller (INTC) is located ahead of RV55 VIC to provide flexibility in handling interrupt requests. SCP clock controller also needs the Sleep IRQ to trigger clock resume finite-state machine. There are four features shown as below and the block diagram is illustrated in Figure 3-3.

- Enable/Disable (Mask) control for each interrupt request
  Management of valid interrupt
- Configure interrupt polarity
  Change the interrupt polarity to meet the polarity requirement of RV55
- Synchronize the interrupt signal to RV55 clock domain
  Solve the clock domain crossing issue of interrupt signals
- Group module groups irqs to 16 groups, which will be triggered to RV55 VIC

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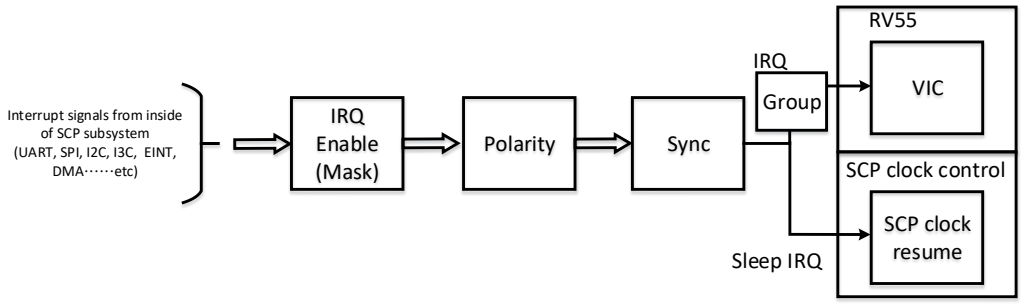

Figure 3-3 INTC block diagram

3.5.8.2 Interrupt Source

Interrupt signals for INTC module are listed in Table 3-4.

Table 3-4 IRQ table

NVIC No.	Interrupt source
0	scp_gipc_in_0
1	scp_gipc_in_1
2	scp_gipc_in_2
3	scp_gipc_in_3
4	spm2scp_irq
5	scp_cirq_event_b
6	eint_irq_core0/1
7	pmic2scp_irq
8	irq_b_u_UART
9	irq_b_u_UART1
10	irq_b_u_I3C0
11	irq_b_u_I2C0
12	TSIP_AXI_tracker_bus_dbg_tracker_irq_b
13	clk_ctrl_irq_u_CLK_CTRL
14	data_valid_irq_u_VOWIF
15	timer0_irq_u_scp_timer_core0/1
16	timer1_irq_u_scp_timer_core0/1
17	timer2_irq_u_scp_timer_core0/1
18	timer3_irq_u_scp_timer_core0/1
19	timer4_irq_u_scp_timer_core0/1
20	timer5_irq_u_scp_timer_core0/1
21	os_timer_irq_u_scp_timer_core0/1
22	uart_rx_irq_core0/1
23	uart1_rx_irq_core0/1
24	dma_irq_b_core0/1
25	scp_audio_irq_b
26	scp_misc_irq_in_vdec_int_line_cnt_irq_b
27	adsp_irq_b
28	cpu_tick_irq_u_scp_timer_core0/1

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NVIC No.	Interrupt source
29	spi0_irq_b
30	spi1_irq_b
31	spi2_irq_b
32	new_infra_sys_cirq_b
33	dbg_irq
34	scp_misc_irq_in_gce_irq_b
35	scp_misc_irq_in_mdp_gce_irq_b
36	scp_misc_irq_in_vdec_irq_b
37	wdt_irq_core0/1
38	scp_misc_irq_in_vdec_lat_irq_b
39	gce_secure_irq_b
40	gce1_secure_irq_b
41	scp_infra_irq
42	clk_ctrl_irq_core0_u_CLK_CTRL
43	clk_ctrl_irq_2_core0_u_CLK_CTRL
44	clk_ctrl_irq_2_u_CLK_CTRL
45	scp_gipc_in_4
46	peribus_timeout_irq
47	infrabus_timeout_irq
48	scp_met_irq[0]
49	scp_met_irq[1]
50	scp_met_irq[2]
51	scp_met_irq[3]
52	ap_wdt_event
53	l2tcm_sec_vio
54	cpu_tick1_irq_u_scp_timer_core0
55	vow_data_in_irq
56	i3c0_ibi_wake
57	i2c0_ibi_wake
58	scp_misc_irq_in_venc_irq_b
59	apu_engine_irq
60	mbox_irq_0
61	mbox_irq_1
62	mbox_irq_2
63	mbox_irq_3
64	mbox_irq_4
65	clk_sys_req_irq_core0/1
66	bus_req_irq_core0/1
67	apsrc_req_irq_core0/1
68	apu2scp_mbox_irq
69	devapc_TSIP_AO_wrapper_secure_vio_irq_b
70	scp_misc_irq_in_camsys_irq_b_29

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NVIC No.	Interrupt source
71	scp_misc_irq_in_camsys_irq_b_28
72	scp_misc_irq_in_camsys_irq_b_5
73	scp_misc_irq_in_camsys_irq_b_4
74	scp_misc_irq_in_camsys_irq_b_3
75	scp_misc_irq_in_camsys_irq_b_2
76	smi_larb7_irq_b_x1
77	wpe_vpp0_wpe_int_b_x1
78	dp_tx_irq
79	edp_tx_irq
80	vpp0_irq_b[0]
81	vpp0_irq_b[12]
82	vpp0_irq_b[14]
83	msdc2_irq_b
84	scp_misc_irq_jpegenc_irq_b
85	scp_misc_irq_jpegdec_irq_b
86	scp_misc_irq_hdmitx_int_x
87	scp_misc_irq_cec_int
88	i2c_irqb[7]
89	i2c_irqb[8]
90	i2c_irqb[9]
91	i2c_irqb[10]
92	i2c_irqb[11]
93	i2c_irqb[12]
94	i2c_irqb[13]
95	infra_iommu_slow_bank0
96	infra_iommu_slow_bank1
97	infra_iommu_slow_bank2
98	infra_iommu_slow_bank3
99	infra_iommu_slow_bank4
100	vdo0_top_irq_b_x1[0] (ovl0)
101	vdo0_top_irq_b_x1[1] (wdma0)
102	vdo0_top_irq_b_x1[2] (rdma0)
103	vdo0_top_irq_b_x1[8] (dsi0)
104	vdo0_top_irq_b_x1[9] (dsc_core0)
105	vdo0_top_irq_b_x1[18] (dsi1)
106	vdo0_top_irq_b_x1[19] (dsc_core1)
107	vdo0_top_irq_b_x1[21] (dpintf0)
108	vdo0_top_irq_b_x1[22] (mutex)
109	mmsys_top_irq_b_x1[0] (mutex)
110	mmsys_top_irq_b_x1[1] (rdma0)
111	mmsys_top_irq_b_x1[2] (rdma1)
112	mmsys_top_irq_b_x1[5] (rdma4)

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NVIC No.	Interrupt source
113	mmsys_top_irq_b_x1[6] (rdma5)
114	mmsys_top_irq_b_x1[25] (merge4)
115	mmsys_top_irq_b_x1[29] (dpi0)
116	mmsys_top_irq_b_x1[30] (dpi1)
117	mmsys_top_irq_b_x1[31] (dpintf)
118	vppsys1_irq_b_x1[8] (rdma2)
119	vppsys1_irq_b_x1[9] (rdma3)
120	vppsys1_irq_b_x1[32] (wrot2)
121	vppsys1_irq_b_x1[33] (wrot3)
122	vppsys1_irq_b_x1[37] (mutex)

3.5.8.3 INTC Programming Outline

Table 3-5 INTC programming outline

Step	Sequence	REG_Name	REG_Value	Address
1	Change IRQ polarity if needed	IRQ_CTRL_POL	User defined	SCP/AP Base Address + 0x32030/0x32034/0x32038/0x3203C
2-1	Enable IRQ to RV55	IRQ_CTRL_EN	User defined	SCP/AP Base Address + 0x32020/0x32024/0x32028/0x3202C
2-2	Enable IRQ as RV55 wakeup event	IRQ_CTRL_SLP	User defined	SCP/AP Base Address + 0x32040/0x32044/0x32048/0x3204C
2-3	Group IRQs as RV55 IRQ (16 groups)	IRQ_CTRL_GRP	User defined	SCP/AP Base Address + 0x32080 ~ 0x3217C

3.5.8.4 External Interrupt Controller (EINT)

There are eight shared multi-function pins, which can be programmed as the external interrupt sensing pins for connecting external triggering signals to SCP EINT module. There are de-bounce (anti-glitch) and edge detection functions used to stabilize the external interrupt source, which are located ahead of INTC. The block diagram is illustrated in Figure 3-4.

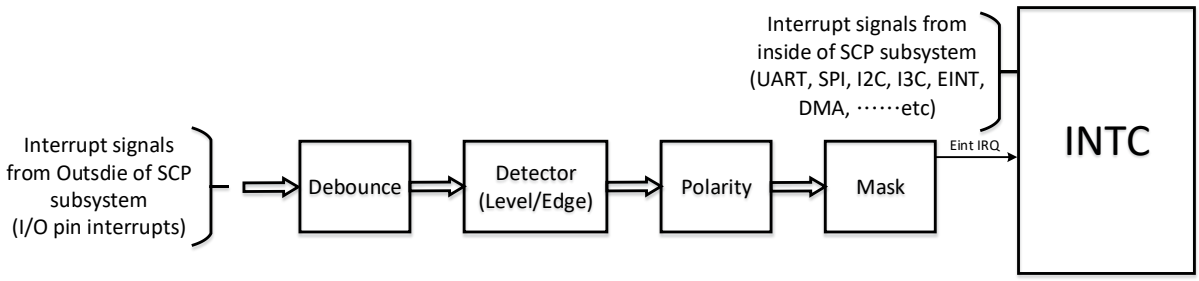

Figure 3-4 EINT block diagram

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3.5.8.5 EINT Programming Outline

Table 3-6 EINT programming outline

Step	Sequence	REG_Name	REG_Value	Address
1	Change the pinmux function mode to support SCP_EINT	N/A	N/A	N/A
2	Change EINT input polarity if needed	EINT_POL_SET	User defined	SCP/AP Base Address + 0x2D340
3-1	Select which EINT input will be OR to RV55 core0	EINT_D0EN	User defined	SCP/AP Base Address + 0x2D400
3-2	Select which EINT input will be OR to RV55 core1	EINT_D1EN	User defined	SCP/AP Base Address + 0x2D420
4	Set each EINT input de-bounce	EINT_DBNC_SET	User defined	SCP/AP Base Address + 0x2D600 ~ SCP/AP Base Address + 0x2D61C
5	Enable EINT input	EINT_MASK_CLR	User defined	SCP/AP Base Address + 0x2D100

3.5.9 Timer

Timer is a countdown counter whose time intervals are programmable. Users can set the counter's initial value. When the timer counts to zero, it will trigger a time out interrupt to inform RV55. The block diagram is shown in Figure 3-5.

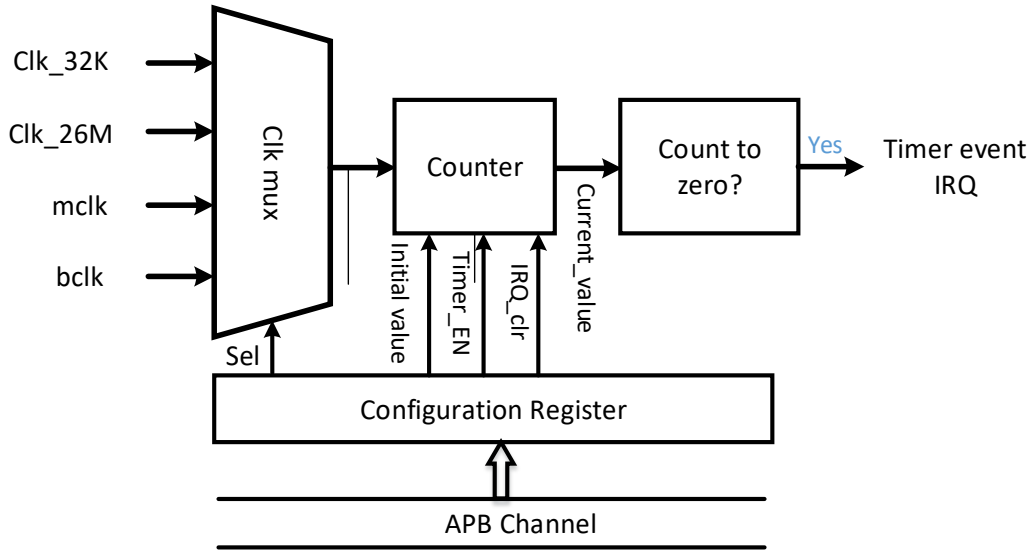

Figure 3-5 SCP timer block diagram

Users can select different clock sources (32 kHz, 26 MHz mclk and bclk) to determine the clock period. Moreover, users can set the counter's initial value to create time interval. When the timer finishes setting up, RV55 can enable the timer to start the counter. The waveform is shown in Figure 3-6.

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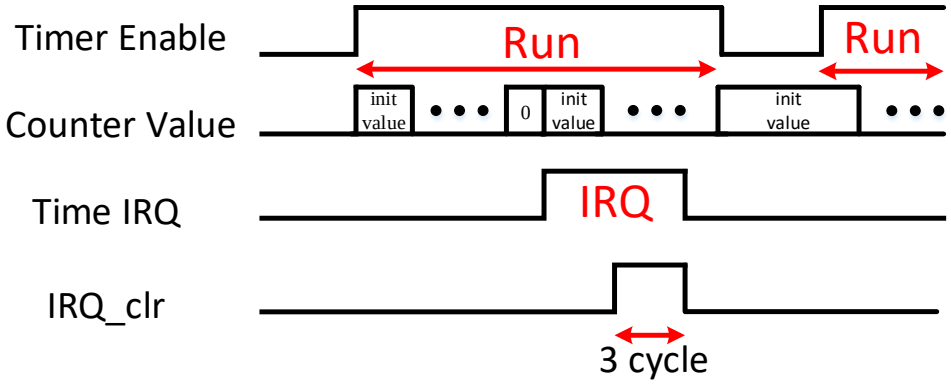

Figure 3-6 SCP timer interrupt event

While the counter counts to the zero, timer will trigger interrupt signal to inform RV55. RV55 needs to give an interrupt clear command to clear interrupt status. Timer is an auto-repeat mode counter. If users want to stop the timer, RV55 needs to give a timer disable command.

3.5.9.1 Timer Programming Outline

Table 3-7 Timer programming outline

Step	Sequence	REG_Name	REG_Value	Address
1	Disable timer and select the clock source	TIMERn_EN	Bit[5:4] = User defined Bit[0] = 1'b0	Core0: SCP/AP Base Address + 0x330n0 Core1: SCP/AP Base Address + 0x430n0
2	Set timer reset value	TIMERn_RST_VAL	User defined	Core0: SCP/AP Base Address + 0x330n4 Core1: SCP/AP Base Address + 0x430n4
3	Set timer IRQ enable	TIMERn_IRQ_CTRL	Bit[0] = 1'b1	Core0: SCP/AP Base Address + 0x330nC Core1: SCP/AP Base Address + 0x430nC
4	Enable timer	TIMERn_EN	Bit[0] = 1'b1	Core0: SCP/AP Base Address + 0x330n0 Core1: SCP/AP Base Address + 0x430n0
5	Set timer IRQ clear	TIMERn_CLR	Bit[5] = 1'b1	Core0: SCP/AP Base Address + 0x330nC Core1: SCP/AP Base Address + 0x430nC
6	Disable timer	TIMERn_EN	Bit[0] = 1'b0	Core0: SCP/AP Base Address + 0x330n0 Core1: SCP/AP Base Address + 0x430n0
7	Repeat Step 4-6			

3.5.10 WDT

A Watchdog Timer (WDT) is an electronic timer that is used to detect RV55 malfunctions. During normal operation, the RV55 regularly resets the watchdog timer to prevent it from "timing out". If, due to a hardware fault or program error, the RV55 fails to reset the watchdog, the timer will elapse and generate a timeout interrupt to inform APMCU that RV55 should stop working. Then, APMCU may trigger a software reset to place RV55 in a safe state and restore normal system operation. The block diagram is shown in Figure 3-7.

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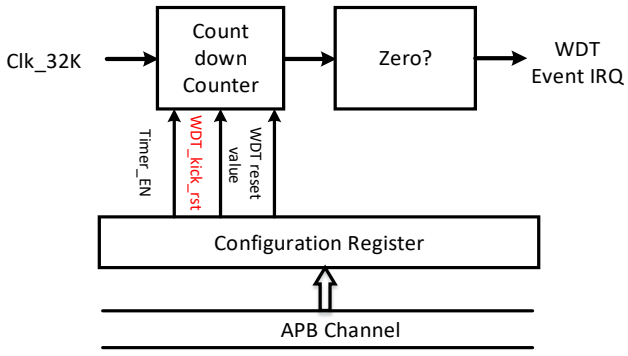

Figure 3-7 SCP WDT block diagram

The purpose of enabling APMCU and setting up SCP WDT is that the APMCU needs to detect the malfunction of RV55. In order to prevent the WDT from triggering an interrupt, RV55 needs to reset (WDT_kick_rst) WDT counter periodically.

3.5.10.1 Watchdog Timer Programming Outline

Table 3-8 WDT programming outline

Step	Sequence	REG_Name	REG_Value	Address
1	Enable WDT and set the reset counter value	WDT_CFG	User defined	SCP/AP Base Address + 0x30034
2	RV55 kicks WDT reset periodically	WDT_KICK	User defined	SCP/AP Base Address + 0x30038
3	If WDT is triggered, APMCU clears the WDT irq and resets SCP.	WDT_IRQ	User defined	SCP/AP Base Address + 0x30030

3.5.11 Semaphore

In SCP, a register-based semaphore is designed for shared resource management between two masters (APMCU and RV55). In real applications, the two masters (APMCU and RV55) may need to use a shared resource (e.g. I2C port in SCP), and users can use this register-based semaphore for privilege management over the shared resources. A master can have access to the shared resource after it takes the semaphore successfully. A master should release the taken semaphore after it finishes the control on the shared resource. As shown in Figure 3-8, there are a total of 16-bit assigned fields for source permission check. For example, suppose that bit 0 is defined as UART0 source permission. The RV55 can write a flag (1'b1) to R_SEMA_H[0] if R_SEMA_M[0] is 1'b0. Otherwise, semaphore hardware does not allow RV55 to set R_SEMA_H[0] as 1'b1. This process is to ensure that there will be no overlap in resource allocation.

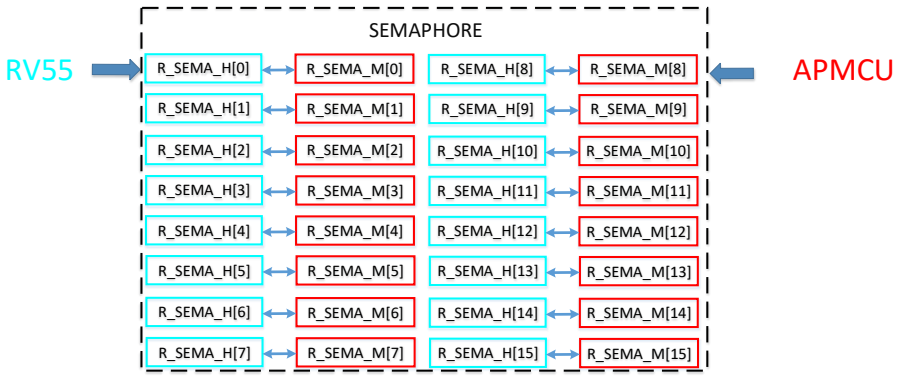

Figure 3-8 Semaphore block diagram

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3.5.12 GPIO

Please refer to Chapter GPIO.

3.5.12.1 GPIO Programming Outline

Table 3-9 GPIO programming outline

Step	Sequence	REG_Name	REG_Value	Address
1	Change the pinmux function mode to support SCP_GPIO	NA	NA	NA
2	Write the data to GPIO_OUT register	SCP_GPIO_OUT	User defined	SCP/AP Base Address + 0x25004
3	Change the IO direction to output	SCP_GPIO_DIR	16'hFFFF	SCP/AP Base Address + 0x25000
4	Change the IO direction to input to get the external data	SCP_GPIO_DIR	16'h0	SCP/AP Base Address + 0x25000
5	Read the data from GPIO_IN register	SCP_GPIO_IN	User defined	SCP/AP Base Address + 0x25008

3.5.13 UART

Please refer to Section 3.12.2 Universal Asynchronous Receiver/Transmitter (UART).

3.5.14 I2C and I3C

Please refer to Section 3.12.1 Inter-Integrated Circuit (I2C) and Improved I2C (I3C).

3.5.15 SPI Master

Please refer to Section 3.12.3 Serial Peripheral Interface (SPI).

3.5.16 Memory Map of SCP Sub-system

The memory map of SCP sub-system is shown in Table 3-10. Except areas of L2TCM, SCP registers and Private Peripheral Bus (PPB), devices in other addressing areas are actually outside of SCP modules and they will need further address remapping and device APC setting (for security access) to be reached by SCP. With the help of remapping logic, the MSB [31:28] of addressing value can be extended from 4-bit to 7-bit in width- so that the SCP can access external devices (e.g. other peripheral devices). Detailed definition and examples of the re-mapping control registers are shown in Section 3.5.16.1 System Address Map from SCP View.

Table 3-10 SCP memory map

Devices	SCP (RV55) view Memory map address		AP view Memory map address	
L2TCM 1MB	0x0000_0000	0x000F_FFFF	0x1050_0000	0x105F_FFFF
ADSP-shared SRAM	0x0010_0000	0x001F_FFFF	NA	
EMI external remap	0x0020_0000	0x002F_FFFF	0x0_4020_0000	0x0_402F_FFFF
EMI external remap	0x0030_0000	0x003F_FFFF	0x0_4030_0000	0x0_403F_FFFF
EMI external remap	0x0040_0000	0x004F_FFFF	0x0_4040_0000	0x0_404F_FFFF
EMI external remap	0x0050_0000	0x005F_FFFF	0x0_4050_0000	0x0_405F_FFFF
EMI external remap	0x0060_0000	0x006F_FFFF	0x0_4060_0000	0x0_406F_FFFF
EMI external remap	0x0070_0000	0x007F_FFFF	0x0_4070_0000	0x0_407F_FFFF

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Devices	SCP (RV55) view Memory map address		AP view Memory map address	
EMI external remap	0x0080_0000	0x0FFF_FFFF	0x0_4080_0000	0x0_4FFF_FFFF
INFRA external bus	0x1000_0000	0x104F_FFFF	NA	
L2TCM 1MB backup	0x1050_0000	0x105F_FFFF	NA	
ADSP-shared SRAM backup	0x1060_0000	0x106B_FFFF	NA	
Reserved	0x1070_0000	0x1071_FFFF	NA	
tmbist_ctrl	0x1072_1000	0x1072_1FFF	0x1072_1000	0x1072_1FFF
SCP Clock ctrl	0x1072_2000	0x1072_2FFF	0x1072_2000	0x1072_2FFF
SCP pmic_wrap_p2p	0x1072_3000	0x1072_3FFF	0x1072_3000	0x1072_3FFF
VOWIF	0x1072_4000	0x1072_4FFF	0x1072_4000	0x1072_4FFF
SCP_CFGREG	0x1072_5000	0x1072_5FFF	0x1072_5000	0x1072_5FFF
GPIO	0x1072_6000	0x1072_6FFF	0x1072_6000	0x1072_6FFF
UART0	0x1072_7000	0x1072_7FFF	0x1072_7000	0x1072_7FFF
UART1	0x1072_8000	0x1072_8FFF	0x1072_8000	0x1072_8FFF
I3C0	0x1072_9000	0x1072_9FFF	0x1072_9000	0x1072_9FFF
I2C0	0x1072_A000	0x1072_AFFF	0x1072_A000	0x1072_AFFF
SPI0	0x1072_B000	0x1072_BFFF	0x1072_B000	0x1072_BFFF
SPI1	0x1072_C000	0x1072_CFFF	0x1072_C000	0x1072_CFFF
SPI2	0x1072_D000	0x1072_DFFF	0x1072_D000	0x1072_DFFF
EINT	0x1072_E000	0x1072_FFFF	0x1072_E000	0x1072_FFFF
Reserved	0x1073_0000	0x1073_0FFF	0x1073_0000	0x1073_0FFF
SCP_CFGREG_CORE0	0x1073_1000	0x1073_1FFF	0x1073_1000	0x1073_1FFF
SCP_DMA_CORE0	0x1073_2000	0x1073_2FFF	0x1073_2000	0x1073_2FFF
SCP_INTC_CORE0	0x1073_3000	0x1073_3FFF	0x1073_3000	0x1073_3FFF
SCP_TIMER_CORE0	0x1073_4000	0x1073_4FFF	0x1073_4000	0x1073_4FFF
Debug APB CORE0	0x1073_5000	0x1073_FFFF	0x1073_5000	0x1073_FFFF
Reserved	0x1074_0000	0x1074_0FFF	0x1074_0000	0x1074_0FFF
SCP_CFGREG_CORE1	0x1074_1000	0x1074_1FFF	0x1074_1000	0x1074_1FFF
SCP_DMA_CORE1	0x1074_2000	0x1074_2FFF	0x1074_2000	0x1074_2FFF
SCP_INTC_CORE1	0x1074_3000	0x1074_3FFF	0x1074_3000	0x1074_3FFF
SCP_TIMER_CORE1	0x1074_4000	0x1074_4FFF	0x1074_4000	0x1074_4FFF
Debug APB CORE1	0x1075_0000	0x1075_0FFF	0x1075_0000	0x1075_0FFF
Main bus bcrm	0x1075_1000	0x1075_1FFF	0x1075_1000	0x1075_1FFF
Main bus debug	0x1075_2000	0x1075_2FFF	0x1075_2000	0x1075_2FFF
Bus tracker	0x1075_3000	0x1075_FFFF	0x1075_3000	0x1075_FFFF
Reserved	0x1076_0000	0x1077_FFFF	0x1076_0000	0x1077_FFFF
CORE0 I/D cache ram (Debug)	0x1078_0000	0x1079_FFFF	0x1078_0000	0x1079_FFFF
CORE1 I/D cache ram (Debug)	0x107A_0000	0x107A_3FFF	0x107A_0000	0x107A_3FFF
Main bus DEVAPCAO	0x107A_4000	0x107A_4FFF	0x107A_4000	0x107A_4FFF
Main bus DEVAPC	0x107A_5000	0x107A_5FFF	0x107A_5000	0x107A_5FFF
SCP_CFGREG_SEC	0x107A_6000	0x107F_A000	0x107A_6000	0x107F_A000
Reserved	0x107F_B000	0x107F_BFFF	0x107F_B000	0x107F_BFFF

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Devices	SCP (RV55) view Memory map address		AP view Memory map address	
SCP MailBox0	0x107F_C000	0x107F_CFFF	0x107F_C000	0x107F_CFFF
SCP MailBox1	0x107F_D000	0x107F_DFFF	0x107F_D000	0x107F_DFFF
SCP MailBox2	0x107F_E000	0x107F_EFFF	0x107F_E000	0x107F_EFFF
SCP MailBox3	0x107F_F000	0x107F_FFFF	0x107F_F000	0x107F_FFFF
SCP MailBox4	0x1072_1000	0x1072_1FFF	0x1072_1000	0x1072_1FFF
INFRA external bus	0x1080_0000	0x1FFF_FFFF	0x1080_0000	0x1FFF_FFFF

3.5.16.1 System Address Map from SCP View

The system address map from SCP view can be configured by some register settings.

Table 3-11 System address map from SCP view

SCP view address [31:28]	Remap register	
	Name	Address
4'h2	REMAP_CFG2::EXT_ADDR2 (Default remap to 0x1)	SCP Base address+0xA506C[6:0]
4'h3	REMAP_CFG2::EXT_ADDR3 (Default remap to 0x1)	SCP Base address+0xA506C[6:0]
4'h4	REMAP_CFG0::EXT_ADDR4 (Default remap to 0x4)	SCP Base address+0xA5064[6:0]
4'h5	REMAP_CFG0::EXT_ADDR5 (Default remap to 0x5)	SCP Base address+0xA5064[14:8]
4'h6	REMAP_CFG0::EXT_ADDR6 (Default remap to 0x6)	SCP Base address+0xA5064[22:16]
4'h7	REMAP_CFG0::EXT_ADDR7 (Default remap to 0x7)	SCP Base address+0xA5064[30:24]
4'h8	REMAP_CFG1::EXT_ADDR8 (Default remap to 0x8)	SCP Base address+0xA5068[6:0]
4'h9	REMAP_CFG1::EXT_ADDR9 (Default remap to 0x9)	SCP Base address+0xA5068[14:8]
4'hA	REMAP_CFG1::EXT_ADDRA (Default remap to 0xA)	SCP Base address+0xA5068[22:16]
4'hB	REMAP_CFG1::EXT_ADDRB (Default remap to 0x0)	SCP Base address+0xA5068[30:24]
4'hC	REMAP_CFG2::EXT_ADDRC (Default remap to 0x1)	SCP Base address+0xA506C[6:0]
4'hD	REMAP_CFG2::EXT_ADDRD (Default remap to 0x2)	SCP Base address+0xA506C[14:8]
4'hE	REMAP_CFG2::EXT_ADDRE (Default remap to 0x3)	SCP Base address+0xA506C[22:16]

Examples: If users want to use SCP view "0xExxx_xxxx" to access AP view "0x3xxx_xxxx", please set REMAP_CFG2::EXT_ADDRE (SCP Base address+0xA506C[22:16]) as 0x3. It means that SCP real access address is "0x3xxx_xxxx" instead of "0xExxx_xxxx" area.

3.6 Memory

The device connects to external memories using External Memory Interface (EMI) controller and two Dynamic Random-Access Memory Controllers (DRAMC) with DDR PHY.

EMI is a sophisticated communication interface before DRAMC and external memories. The EMI controller processes requests from multiple device masters and issues commands to the DRMAC.

There are two EMI controllers. Each has the following key features:

- Prevents DRAM stall, data overflow, and underflow
- Allows gating its own clock when idle
- Connection to two DRAMCs
- Command schedule options:

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  - Starvation control
  - Bandwidth regulator
  - Latency regulator
  - High priority
  - Page hit control
  - Read and write turn around prevent control
  - Memory protection unit (DRAM and APB)
- Dedicated AXI connection ports:
  - 2 × 128-bit read and write ports to the MCUSYS
  - 2 × 128-bit read and write ports to the multimedia modules
  - 2 × 128-bit read and write ports to the APU
  - 1 × 128-bit read and write port to the peripherals

Each DRAMC processes EMI commands and controls the external memory and has the following key features:

- Contains integrated DDR PHY
- Supports the following DDR memory types:
  - 16-bit LPDDR4(X) at 3733 MT/s
  - 16-bit DDR4 at 3200 MT/s
- Schedules and issues DRAM bus commands
- Keeps the integrity of DRAM bus timings
- Supports power-down and self-refresh for power saving
- Supports clock stop for power saving
- Supports DQS/DQ timing calibration for PVT variation
- Supports read/write command out of order control
- Supports per bank refresh

3.6.1 EMI Signal Descriptions

Table 3-12 and Table 3-13 present EMI signal descriptions.

Table 3-12 EMI signal descriptions (LPDDR4(X))

Signal name	Type	Description	Ball location
EMI0—Calibration Resistor, Reset Output, Voltage Reference			
EMI0_EXTR(1)	AIO	EMI0 DRAM output driving calibration resistor	AT2
EMI0_RESET_N	DO	EMI0 DRAM reset output	AU35
EMI0_TP(2)	AIO	EMI0 DRAM command/address voltage reference	AR3
EMI0 Command/Address Bus—EMI0_CA[5:0]			
EMI0_CA0	DO	EMI0 DRAM command/address output 0	AT22
EMI0_CA1	DO	EMI0 DRAM command/address output 1	AR22
EMI0_CA2	DO	EMI0 DRAM command/address output 2	AM23
EMI0_CA3	DO	EMI0 DRAM command/address output 3	AM22
EMI0_CA4	DO	EMI0 DRAM command/address output 4	AN21
EMI0_CA5	DO	EMI0 DRAM command/address output 5	AP21
EMI0 System Bus—Command, Chip Select, Data Mask, Data Strobe, Clock Signals			
EMI0_CK_T	DO	EMI0 DRAM clock	AM20
EMI0_CK_C	DO	EMI0 DRAM clock invert	AL20

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Signal name	Type	Description	Ball location
EMI0_CKE0	DO	EMI0 DRAM clock enable for rank 0	AU20
EMI0_CKE1	DO	EMI0 DRAM clock enable for rank 1	AT20
EMI0_CS0	DO	EMI0 DRAM chip select for rank 0	AR20
EMI0_CS1	DO	EMI0 DRAM chip select for rank 1	AU22
EMI0_DMI0	DIO	EMI0 DRAM data mask/inversion for DQ[7:0]	AU25
EMI0_DMI1	DIO	EMI0 DRAM data mask/inversion for DQ[15:8]	AU31
EMI0_DQS0_T	DIO	EMI0 DRAM data strobe for DQ[7:0]	AM27
EMI0_DQS0_C	DIO	EMI0 DRAM data strobe invert for DQ[7:0]	AN27
EMI0_DQS1_T	DIO	EMI0 DRAM data strobe for DQ[15:8]	AT32
EMI0_DQS1_C	DIO	EMI0 DRAM data strobe invert for DQ[15:8]	AR32
EMI0 Data Bus—EMI0_DQ[15:0]			
EMI0_DQ0	DIO	EMI0 DRAM data pin 0	AU27
EMI0_DQ1	DIO	EMI0 DRAM data pin 1	AT26
EMI0_DQ2	DIO	EMI0 DRAM data pin 2	AL25
EMI0_DQ3	DIO	EMI0 DRAM data pin 3	AP25
EMI0_DQ4	DIO	EMI0 DRAM data pin 4	AL24
EMI0_DQ5	DIO	EMI0 DRAM data pin 5	AN25
EMI0_DQ6	DIO	EMI0 DRAM data pin 6	AT24
EMI0_DQ7	DIO	EMI0 DRAM data pin 7	AT28
EMI0_DQ8	DIO	EMI0 DRAM data pin 8	AU34
EMI0_DQ9	DIO	EMI0 DRAM data pin 9	AN31
EMI0_DQ10	DIO	EMI0 DRAM data pin 10	AP30
EMI0_DQ11	DIO	EMI0 DRAM data pin 11	AN29
EMI0_DQ12	DIO	EMI0 DRAM data pin12	AR29
EMI0_DQ13	DIO	EMI0 DRAM data pin 13	AP31
EMI0_DQ14	DIO	EMI0 DRAM data pin 14	AT30
EMI0_DQ15	DIO	EMI0 DRAM data pin 15	AU29
EMI1 Command/Address Bus—EMI1_CA[5:0]			
EMI1_CA0	DO	EMI1 DRAM command/address output 0	AT16
EMI1_CA1	DO	EMI1 DRAM command/address output 1	AR16
EMI1_CA2	DO	EMI1 DRAM command/address output 2	AL15
EMI1_CA3	DO	EMI1 DRAM command/address output 3	AP16
EMI1_CA4	DO	EMI1 DRAM command/address output 4	AN16
EMI1_CA5	DO	EMI1 DRAM command/address output 5	AL16
EMI1 System Bus—Command, Chip Select, Data Mask, Data Strobe, Clock Signals			
EMI1_CK_T	DO	EMI1 DRAM clock	AM18
EMI1_CK_C	DO	EMI1 DRAM clock invert	AL18
EMI1_CKE0	DO	EMI1 DRAM clock enable for rank 0	AU18
EMI1_CKE1	DO	EMI1 DRAM clock enable for rank 1	AT18
EMI1_CS0	DO	EMI1 DRAM chip select for rank 0	AR18
EMI1_CS1	DO	EMI1 DRAM chip select for rank 1	AU16
EMI1_DMI0	DIO	EMI1 DRAM data mask/inversion for DQ[7:0]	AU13
EMI1_DMI1	DIO	EMI1 DRAM data mask/inversion for DQ[15:8]	AU7

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Signal name	Type	Description	Ball location
EMI1_DQS0_T	DIO	EMI1 DRAM data strobe for DQ[7:0]	AN11
EMI1_DQS0_C	DIO	EMI1 DRAM data strobe invert for DQ[7:0]	AM11
EMI1_DQS1_T	DIO	EMI1 DRAM data strobe for DQ[15:8]	AU5
EMI1_DQS1_C	DIO	EMI1 DRAM data strobe invert for DQ[15:8]	AT5
EMI1 Data Bus—EMI1_DQ[15:0]			
EMI1_DQ0	DIO	EMI1 DRAM data pin 0	AU11
EMI1_DQ1	DIO	EMI1 DRAM data pin 1	AT12
EMI1_DQ2	DIO	EMI1 DRAM data pin 2	AR11
EMI1_DQ3	DIO	EMI1 DRAM data pin 3	AN13
EMI1_DQ4	DIO	EMI1 DRAM data pin 4	AL13
EMI1_DQ5	DIO	EMI1 DRAM data pin 5	AP13
EMI1_DQ6	DIO	EMI1 DRAM data pin 6	AT14
EMI1_DQ7	DIO	EMI1 DRAM data pin 7	AT10
EMI1_DQ8	DIO	EMI1 DRAM data pin 8	AR4
EMI1_DQ9	DIO	EMI1 DRAM data pin 9	AU4
EMI1_DQ10	DIO	EMI1 DRAM data pin 10	AN8
EMI1_DQ11	DIO	EMI1 DRAM data pin 11	AR9
EMI1_DQ12	DIO	EMI1 DRAM data pin 12	AN9
EMI1_DQ13	DIO	EMI1 DRAM data pin 13	AR6
EMI1_DQ14	DIO	EMI1 DRAM data pin 14	AT8
EMI1_DQ15	DIO	EMI1 DRAM data pin 15	AU9
EMI2—Calibration Resistor, Reset Output, Voltage Reference			
EMI2_EXTR(1)	AIO	EMI2 DRAM output driving calibration resistor	B2
EMI2_RESET_N	DO	EMI2 DRAM reset output	B36
EMI2_TP(2)	AIO	EMI2 DRAM command/address voltage reference	A3
EMI2 Command/Address Bus—EMI2_CA[5:0]			
EMI2_CA0	DO	EMI2 DRAM command/address output 0	B16
EMI2_CA1	DO	EMI2 DRAM command/address output 1	C16
EMI2_CA2	DO	EMI2 DRAM command/address output 2	F15
EMI2_CA3	DO	EMI2 DRAM command/address output 3	F16
EMI2_CA4	DO	EMI2 DRAM command/address output 4	E17
EMI2_CA5	DO	EMI2 DRAM command/address output 5	D17
EMI2 System Bus—Command, Chip Select, Data Mask, Data Strobe, Clock Signals			
EMI2_CK_T	DO	EMI2 DRAM clock	F18
EMI2_CK_C	DO	EMI2 DRAM clock invert	G18
EMI2_CKE0	DO	EMI2 DRAM clock enable for rank 0	A18
EMI2_CKE1	DO	EMI2 DRAM clock enable for rank 1	B18
EMI2_CS0	DO	EMI2 DRAM chip select for rank 0	C18
EMI2_CS1	DO	EMI2 DRAM chip select for rank 1	A16
EMI2_DMI0	DIO	EMI2 DRAM data mask/inversion for DQ[7:0]	A13
EMI2_DMI1	DIO	EMI2 DRAM data mask/inversion for DQ[15:8]	A7
EMI2_DQS0_T	DIO	EMI2 DRAM data strobe for DQ[7:0]	F11
EMI2_DQS0_C	DIO	EMI2 DRAM data strobe invert for DQ[7:0]	E11

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Signal name	Type	Description	Ball location
EMI2_DQS1_T	DIO	EMI2 DRAM data strobe for DQ[15:8]	B6
EMI2_DQS1_C	DIO	EMI2 DRAM data strobe invert for DQ[15:8]	C6
EMI2 Data Bus—EMI2_DQ[15:0]			
EMI2_DQ0	DIO	EMI2 DRAM data pin 0	A11
EMI2_DQ1	DIO	EMI2 DRAM data pin 1	B12
EMI2_DQ2	DIO	EMI2 DRAM data pin 2	G13
EMI2_DQ3	DIO	EMI2 DRAM data pin 3	D13
EMI2_DQ4	DIO	EMI2 DRAM data pin 4	G14
EMI2_DQ5	DIO	EMI2 DRAM data pin 5	E13
EMI2_DQ6	DIO	EMI2 DRAM data pin 6	B14
EMI2_DQ7	DIO	EMI2 DRAM data pin 7	B10
EMI2_DQ8	DIO	EMI2 DRAM data pin 8	A4
EMI2_DQ9	DIO	EMI2 DRAM data pin 9	E7
EMI2_DQ10	DIO	EMI2 DRAM data pin 10	D8
EMI2_DQ11	DIO	EMI2 DRAM data pin 11	E9
EMI2_DQ12	DIO	EMI2 DRAM data pin 12	C9
EMI2_DQ13	DIO	EMI2 DRAM data pin 13	D7
EMI2_DQ14	DIO	EMI2 DRAM data pin 14	B8
EMI2_DQ15	DIO	EMI2 DRAM data pin 15	A9
EMI3 Command/Address Bus—EMI3_CA[5:0]			
EMI3_CA0	DO	EMI3 DRAM command/address output 0	B22
EMI3_CA1	DO	EMI3 DRAM command/address output 1	C22
EMI3_CA2	DO	EMI3 DRAM command/address output 2	G23
EMI3_CA3	DO	EMI3 DRAM command/address output 3	D22
EMI3_CA4	DO	EMI3 DRAM command/address output 4	E22
EMI3_CA5	DO	EMI3 DRAM command/address output 5	G22
EMI3 System Bus—Command, Chip Select, Data Mask, Data Strobe, Clock Signals			
EMI3_CK_T	DO	EMI3 DRAM clock	F20
EMI3_CK_C	DO	EMI3 DRAM clock invert	G20
EMI3_CKE0	DO	EMI3 DRAM clock enable for rank 0	A20
EMI3_CKE1	DO	EMI3 DRAM clock enable for rank 1	B20
EMI3_CS0	DO	EMI3 DRAM chip select for rank 0	C20
EMI3_CS1	DO	EMI3 DRAM chip select for rank 1	A22
EMI3_DMI0	DIO	EMI3 DRAM data mask/inversion for DQ[7:0]	A25
EMI3_DMI1	DIO	EMI3 DRAM data mask/inversion for DQ[15:8]	A31
EMI3_DQS0_T	DIO	EMI3 DRAM data strobe for DQ[7:0]	E27
EMI3_DQS0_C	DIO	EMI3 DRAM data strobe invert for DQ[7:0]	F27
EMI3_DQS1_T	DIO	EMI3 DRAM data strobe for DQ[15:8]	A33
EMI3_DQS1_C	DIO	EMI3 DRAM data strobe invert for DQ[15:8]	B33
EMI3 Data Bus—EMI3_DQ[15:0]			
EMI3_DQ0	DIO	EMI3 DRAM data pin 0	A27
EMI3_DQ1	DIO	EMI3 DRAM data pin 1	B26
EMI3_DQ2	DIO	EMI3 DRAM data pin 2	C27

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Signal name	Type	Description	Ball location
EMI3_DQ3	DIO	EMI3 DRAM data pin 3	E25
EMI3_DQ4	DIO	EMI3 DRAM data pin 4	G25
EMI3_DQ5	DIO	EMI3 DRAM data pin 5	D25
EMI3_DQ6	DIO	EMI3 DRAM data pin 6	B24
EMI3_DQ7	DIO	EMI3 DRAM data pin 7	B28
EMI3_DQ8	DIO	EMI3 DRAM data pin 8	C34
EMI3_DQ9	DIO	EMI3 DRAM data pin 9	A34
EMI3_DQ10	DIO	EMI3 DRAM data pin 10	E30
EMI3_DQ11	DIO	EMI3 DRAM data pin 11	C29
EMI3_DQ12	DIO	EMI3 DRAM data pin 12	E29
EMI3_DQ13	DIO	EMI3 DRAM data pin 13	C32
EMI3_DQ14	DIO	EMI3 DRAM data pin 14	B30
EMI3_DQ15	DIO	EMI3 DRAM data pin 15	A29

1. Connect this pin through an external 60.4 Ω (1%) resistor to GND.
2. If not used, it can be left unconnected.

Table 3-13 EMI signal descriptions (DDR4)

Signal name	Type	Description	Ball location
EMI0—Calibration Resistor, Reset Output, Voltage Reference			
EMI0_EXTR(1)	AIO	EMI0 DRAM output driving calibration resistor	AT2
EMI0_RESET_N	DO	EMI0 DRAM reset output	AU35
EMI0_TP(2)	AIO	EMI0 DRAM command/address voltage reference	AR3
EMI0 Command/Address Bus—EMI0_CA[13:0]			
EMI0_CA0	DO	EMI0 DRAM command/address output 0	AN16
EMI0_CA1	DO	EMI0 DRAM command/address output 1	AP21
EMI0_CA2	DO	EMI0 DRAM command/address output 2	AL18
EMI0_CA3	DO	EMI0 DRAM command/address output 3	AU22
EMI0_CA4	DO	EMI0 DRAM command/address output 4	AU16
EMI0_CA5	DO	EMI0 DRAM command/address output 5	AM22
EMI0_CA6	DO	EMI0 DRAM command/address output 6	AP16
EMI0_CA7	DO	EMI0 DRAM command/address output 7	AM23
EMI0_CA8	DO	EMI0 DRAM command/address output 8	AL15
EMI0_CA9	DO	EMI0 DRAM command/address output 9	AL22
EMI0_CA10	DO	EMI0 DRAM command/address output 10	AR16
EMI0_CA11	DO	EMI0 DRAM command/address output 11	AK19
EMI0_CA12	DO	EMI0 DRAM command/address output 12	AT22
EMI0_CA13	DO	EMI0 DRAM command/address output 13	AM18
EMI0 System Bus—Command, Chip Select, Data Mask, Data Strobe, Clock Signals			
EMI0_ACT_N	DO	EMI0 DRAM activation command output	AT18
EMI0_BA0	DO	EMI0 DRAM bank address 0	AL16
EMI0_BA1	DO	EMI0 DRAM bank address 1	AN21
EMI0_BG0	DO	EMI0 DRAM bank group 0	AT16
EMI0_CAS_N	DO	EMI0 DRAM column address strobe output	AM15

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Signal name	Type	Description	Ball location
EMI0_CK_T	DO	EMI0 DRAM clock	AM20
EMI0_CK_C	DO	EMI0 DRAM clock invert	AL20
EMI0_CKE0	DO	EMI0 DRAM clock enable for rank 0	AU20
EMI0_CS0	DO	EMI0 DRAM chip select for rank 0	AR20
EMI0_DMI0	DIO	EMI0 DRAM data mask/inversion for DQ[7:0]	AU31
EMI0_DMI1	DIO	EMI0 DRAM data mask/inversion for DQ[15:8]	AU25
EMI0_DQS0_T	DO	EMI0 DRAM data strobe for DQ[7:0]	AM27
EMI0_DQS0_C	DO	EMI0 DRAM data strobe invert for DQ[7:0]	AN27
EMI0_DQS1_T	DO	EMI0 DRAM data strobe for DQ[15:8]	AT32
EMI0_DQS1_C	DO	EMI0 DRAM data strobe invert for DQ[15:8]	AR32
EMI0_ODT(3)	AIO	EMI0 on die termination	AP19
EMI0_RAS_N	DO	EMI0 DRAM row address strobe output	AR22
EMI0_WE_N	DO	EMI0 DRAM write enable output	AT20
EMI0 Data Bus—EMI0_DQ[15:0]			
EMI0_DQ0	DIO	EMI0 DRAM data pin 0	AN25
EMI0_DQ1	DIO	EMI0 DRAM data pin 1	AT28
EMI0_DQ2	DIO	EMI0 DRAM data pin 2	AP25
EMI0_DQ3	DIO	EMI0 DRAM data pin 3	AP30
EMI0_DQ4	DIO	EMI0 DRAM data pin 4	AL24
EMI0_DQ5	DIO	EMI0 DRAM data pin 5	AP31
EMI0_DQ6	DIO	EMI0 DRAM data pin 6	AN29
EMI0_DQ7	DIO	EMI0 DRAM data pin 7	AR29
EMI0_DQ8	DIO	EMI0 DRAM data pin 8	AT26
EMI0_DQ9	DIO	EMI0 DRAM data pin 9	AU34
EMI0_DQ10	DIO	EMI0 DRAM data pin 10	AU27
EMI0_DQ11	DIO	EMI0 DRAM data pin 11	AT30
EMI0_DQ12	DIO	EMI0 DRAM data pin12	AT24
EMI0_DQ13	DIO	EMI0 DRAM data pin 13	AN31
EMI0_DQ14	DIO	EMI0 DRAM data pin 14	AL25
EMI0_DQ15	DIO	EMI0 DRAM data pin 15	AU29
EMI1 System Bus—Command, Chip Select, Data Mask, Data Strobe, Clock Signals			
EMI1_CKE0	DO	EMI1 DRAM clock enable	AU18
EMI1_CS0	DO	EMI1 DRAM chip select	AR18
EMI1_DMI0	DIO	EMI1 DRAM data mask/inversion for DQ[7:0]	AU13
EMI1_DMI1	DIO	EMI1 DRAM data mask/inversion for DQ[15:8]	AU7
EMI1_DQS0_T	DIO	EMI1 DRAM data strobe for DQ[7:0]	AU5
EMI1_DQS0_C	DIO	EMI1 DRAM data strobe invert for DQ[7:0]	AT5
EMI1_DQS1_T	DIO	EMI1 DRAM data strobe for DQ[15:8]	AN11
EMI1_DQS1_C	DIO	EMI1 DRAM data strobe invert for DQ[15:8]	AM11
EMI1 Data Bus—EMI1_DQ[15:0]			
EMI1_DQ0	DIO	EMI1 DRAM data pin 0	AU4
EMI1_DQ1	DIO	EMI1 DRAM data pin 1	AL13
EMI1_DQ2	DIO	EMI1 DRAM data pin 2	AN8

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Signal name	Type	Description	Ball location
EMI1_DQ3	DIO	EMI1 DRAM data pin 3	AN13
EMI1_DQ4	DIO	EMI1 DRAM data pin 4	AR6
EMI1_DQ5	DIO	EMI1 DRAM data pin 5	AP13
EMI1_DQ6	DIO	EMI1 DRAM data pin 6	AN9
EMI1_DQ7	DIO	EMI1 DRAM data pin 7	AR9
EMI1_DQ8	DIO	EMI1 DRAM data pin 8	AU9
EMI1_DQ9	DIO	EMI1 DRAM data pin 9	AR11
EMI1_DQ10	DIO	EMI1 DRAM data pin 10	AT10
EMI1_DQ11	DIO	EMI1 DRAM data pin 11	AT12
EMI1_DQ12	DIO	EMI1 DRAM data pin 12	AT8
EMI1_DQ13	DIO	EMI1 DRAM data pin 13	AT14
EMI1_DQ14	DIO	EMI1 DRAM data pin 14	AR4
EMI1_DQ15	DIO	EMI1 DRAM data pin 15	AU11
EMI2—Calibration Resistor, Reset Output, Voltage Reference			
EMI2_EXTR(1)	AIO	EMI2 DRAM output driving calibration resistor	B2
EMI2_RESET_N	DO	EMI2 DRAM reset output	B36
EMI2_TP(2)	AIO	EMI2 DRAM command/address voltage reference	A3
EMI2 Command/Address Bus—EMI2_CA[13:0]			
EMI2_CA0	DO	EMI2 DRAM command/address output 0	E22
EMI2_CA1	DO	EMI2 DRAM command/address output 1	D17
EMI2_CA2	DO	EMI2 DRAM command/address output 2	G20
EMI2_CA3	DO	EMI2 DRAM command/address output 3	A16
EMI2_CA4	DO	EMI2 DRAM command/address output 4	A22
EMI2_CA5	DO	EMI2 DRAM command/address output 5	F16
EMI2_CA6	DO	EMI2 DRAM command/address output 6	D22
EMI2_CA7	DO	EMI2 DRAM command/address output 7	F15
EMI2_CA8	DO	EMI2 DRAM command/address output 8	G23
EMI2_CA9	DO	EMI2 DRAM command/address output 9	G16
EMI2_CA10	DO	EMI2 DRAM command/address output 10	C22
EMI2_CA11	DO	EMI2 DRAM command/address output 11	H19
EMI2_CA12	DO	EMI2 DRAM command/address output 12	B16
EMI2_CA13	DO	EMI2 DRAM command/address output 13	F20
EMI2 System Bus—Command, Chip Select, Data Mask, Data Strobe, Clock Signals			
EMI2_ACT_N	DO	EMI2 DRAM activation command output	B20
EMI2_BA0	DO	EMI2 DRAM bank address 0	G22
EMI2_BA1	DO	EMI2DRAM bank address 1	E17
EMI2_BG0	DO	EMI2 DRAM bank group 0	B22
EMI2_CAS_N	DO	EMI2 DRAM column address strobe output	F23
EMI2_CK_T	DO	EMI2 DRAM clock	F18
EMI2_CK_C	DO	EMI2 DRAM clock invert	G18
EMI2_CKE0	DO	EMI2 DRAM clock enable	A18
EMI2_CS0	DO	EMI2 DRAM chip select	C18
EMI2_DMI0	DIO	EMI2 DRAM data mask/inversion for DQ[7:0]	A7

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Signal name	Type	Description	Ball location
EMI2_DMI1	DIO	EMI2 DRAM data mask/inversion for DQ[15:8]	A13
EMI2_DQS0_T	DIO	EMI2 DRAM data strobe for DQ[7:0]	F11
EMI2_DQS0_C	DIO	EMI2 DRAM data strobe invert for DQ[7:0]	E11
EMI2_DQS1_T	DIO	EMI2 DRAM data strobe for DQ[15:8]	B6
EMI2_DQS1_C	DIO	EMI2 DRAM data strobe invert for DQ[15:8]	C6
EMI2_ODT[3]	AIO	EMI2 on die termination	D19
EMI2_RAS_N	DO	EMI2 DRAM row address strobe output	C16
EMI2_WE_N	DO	EMI2 DRAM write enable output	B18
EMI2 Data Bus—EMI2_DQ[15:0]			
EMI2_DQ0	DIO	EMI2 DRAM data pin 0	E13
EMI2_DQ1	DIO	EMI2 DRAM data pin 1	B10
EMI2_DQ2	DIO	EMI2 DRAM data pin 2	D13
EMI2_DQ3	DIO	EMI2 DRAM data pin 3	D8
EMI2_DQ4	DIO	EMI2 DRAM data pin 4	G14
EMI2_DQ5	DIO	EMI2 DRAM data pin 5	D7
EMI2_DQ6	DIO	EMI2 DRAM data pin 6	E9
EMI2_DQ7	DIO	EMI2 DRAM data pin 7	C9
EMI2_DQ8	DIO	EMI2 DRAM data pin 8	B12
EMI2_DQ9	DIO	EMI2 DRAM data pin 9	A4
EMI2_DQ10	DIO	EMI2 DRAM data pin 10	A11
EMI2_DQ11	DIO	EMI2 DRAM data pin 11	B8
EMI2_DQ12	DIO	EMI2 DRAM data pin 12	B14
EMI2_DQ13	DIO	EMI2 DRAM data pin 13	E7
EMI2_DQ14	DIO	EMI2 DRAM data pin 14	G13
EMI2_DQ15	DIO	EMI2 DRAM data pin 15	A9
EMI3 System Bus—Command, Chip Select, Data Mask, Data Strobe, Clock Signals			
EMI3_CKE0	DO	EMI3 DRAM clock enable	A20
EMI3_CS0	DO	EMI3 DRAM chip select	C20
EMI3_DMI0	DIO	EMI3 DRAM data mask/inversion for DQ[7:0]	A25
EMI3_DMI1	DIO	EMI3 DRAM data mask/inversion for DQ[15:8]	A31
EMI3_DQS0_T	DIO	EMI3 DRAM data strobe for DQ[7:0]	A33
EMI3_DQS0_C	DIO	EMI3 DRAM data strobe invert for DQ[7:0]	B33
EMI3_DQS1_T	DIO	EMI3 DRAM data strobe for DQ[15:8]	E27
EMI3_DQS1_C	DIO	EMI3 DRAM data strobe invert for DQ[15:8]	F27
EMI3 Data Bus—EMI3_DQ[15:0]			
EMI3_DQ0	DIO	EMI3 DRAM data pin 0	A34
EMI3_DQ1	DIO	EMI3 DRAM data pin 1	G25
EMI3_DQ2	DIO	EMI3 DRAM data pin 2	E30
EMI3_DQ3	DIO	EMI3 DRAM data pin 3	E25
EMI3_DQ4	DIO	EMI3 DRAM data pin 4	C32
EMI3_DQ5	DIO	EMI3 DRAM data pin 5	D25
EMI3_DQ6	DIO	EMI3 DRAM data pin 6	E29
EMI3_DQ7	DIO	EMI3 DRAM data pin 7	C29

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Signal name	Type	Description	Ball location
EMI3_DQ8	DIO	EMI3 DRAM data pin 8	A29
EMI3_DQ9	DIO	EMI3 DRAM data pin 9	C27
EMI3_DQ10	DIO	EMI3 DRAM data pin 10	B28
EMI3_DQ11	DIO	EMI3 DRAM data pin 11	B26
EMI3_DQ12	DIO	EMI3 DRAM data pin 12	B30
EMI3_DQ13	DIO	EMI3 DRAM data pin 13	B24
EMI3_DQ14	DIO	EMI3 DRAM data pin 14	C34
EMI3_DQ15	DIO	EMI3 DRAM data pin 15	A27

1. Connect this pin through an external 100 Ω(%1) resistor to GND.
2. If not used, it can be left unconnected.
3. Connect this pin to 1/2 AVDDQ_EMI0.

3.6.2 DDR4 Interface

3.6.2.1 DDR4 Timing Characteristics

The EMI DDR4 timing characteristics are compliant with JEDEC Standard—JESD79-4C.

3.6.2.2 DDR4 Application Guidelines

Table 3-14 presents supported DDR4 device combinations.

Table 3-14 DDR4 device combinations

Number of devices	Device data width	Mirrored	EMI width
4	1 × 16 bit	No	64-bit

Figure 3-9 shows the schematic connections for a 64-bit interface using 4×16-bit devices.

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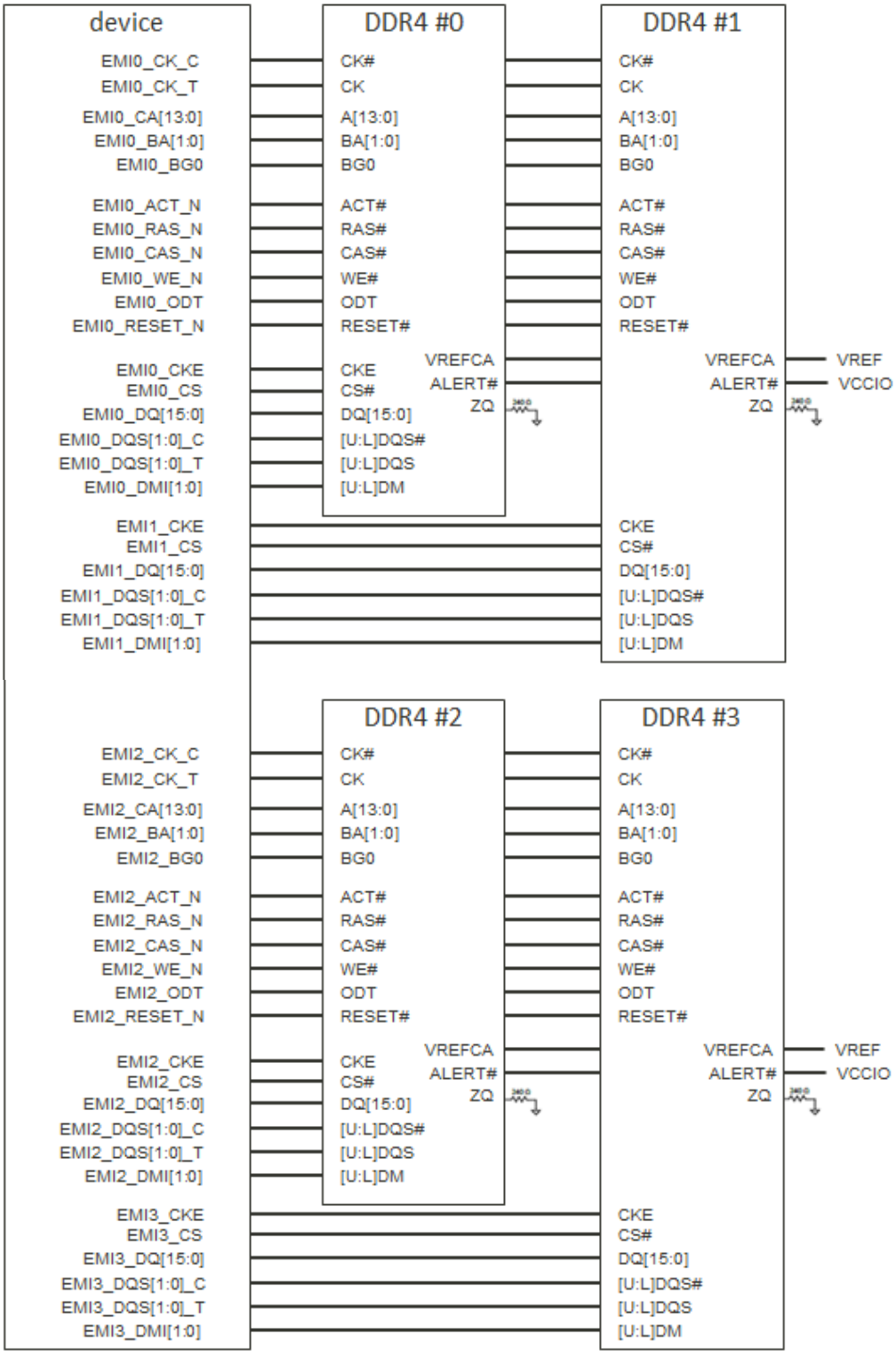

Figure 3-9 DDR4 basic schematic for 4 × 1 × 16-bit

3.6.3 LPDDR4(X) Interface

3.6.3.1 LPDDR4(X) Timing Characteristics

The EMI LPDDR4(X) timing characteristics are compliant with JEDEC Standard—JESD209-4D.

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3.6.3.2 LPDDR4(X) Application Guidelines

Table 3-15 presents supported LPDDR4(X) device combinations.

Table 3-15 LPDDR4(X) device combinations

Number of devices	Device data width	Mirrored	EMI width
2	2 × 16-bit	No	64-bit

Figure 3-10 shows the schematic connections for a 64-bit interface using 2 × 2 ×16-bit devices.

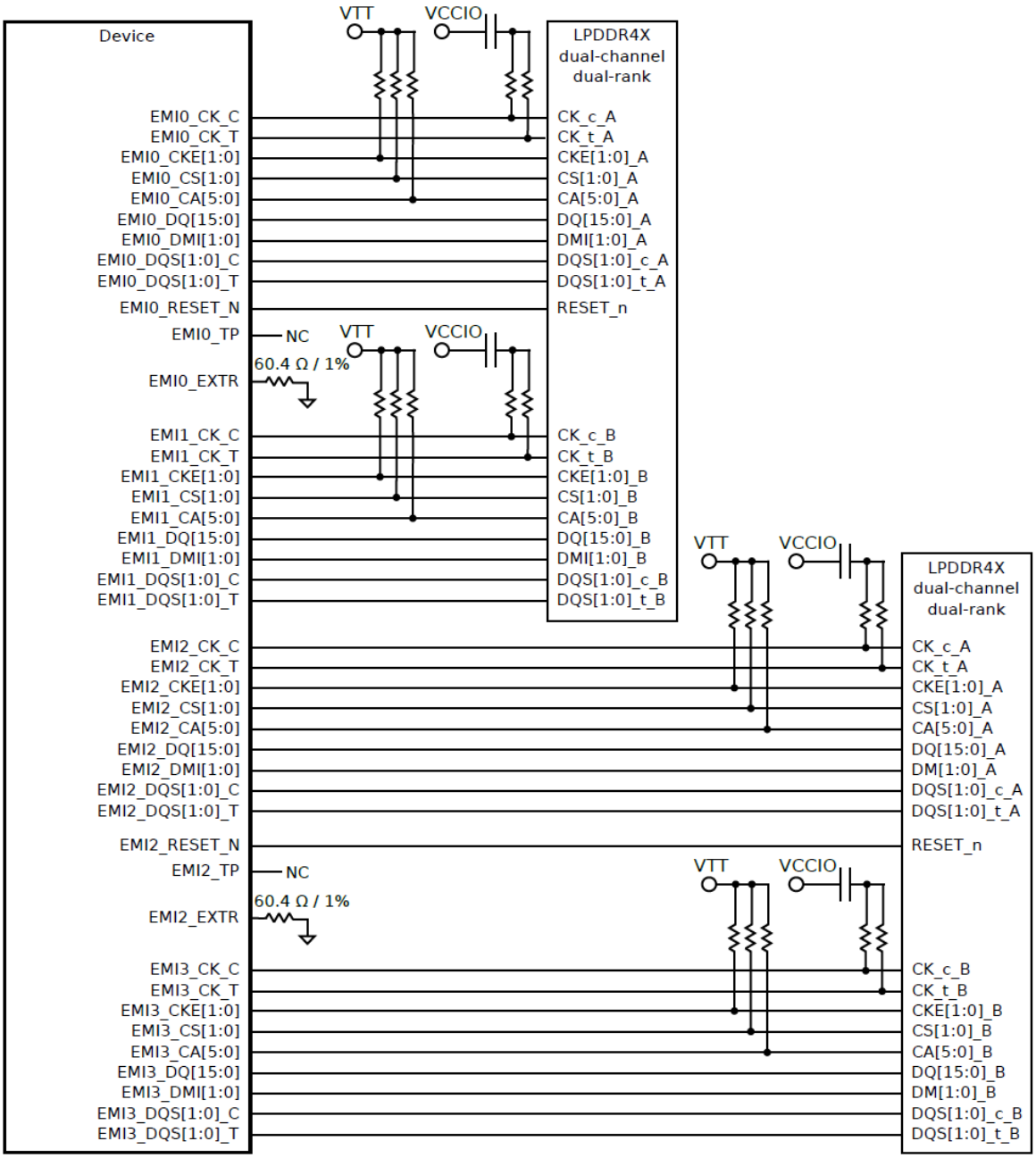

Figure 3-10 LPDDR4(X) basic schematic for 2 × 2 × 16-bit

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3.7 Storage

3.7.1 Memory Card Controller (MSDC)

The Memory Stick and Secure Digital (SD®) card Controller (MSDC) offers a high throughput data transfers while considering power consumption and data security between device local hosts and memory cards.

The MSDC interface fully supports:

- SD3.0 (Secure Digital) memory card specification
- SDIO 3.0 (Secure Digital Input Output) card specification
- eMMC 5.1 (embedded MultiMediaCard) specification

The device has integrated 3 MSDC controllers with the following data bus width:

- MSDC0 is used as eMMC interface
- MSDC1 is used as SD/SDIO interface
- MSDC2 is used as SD/SDIO interface.

Each MSDC module supports the following key features:

- 32-bit access on AHB bus for control registers
- Basic DMA and linked-list based DMA modes

The MSDC0 controller fully supports:

- 64-bit data access on AXI bus
- 1-, 4-, 8-bit data bus width for eMMC
- Backwards compatibility with legacy MMC card
- High-speed Single Data Rate (SDR) mode
- High-speed Dual Data Rate (DDR) mode
- HS200 mode, SDR up to 200 MBps
- HS400 mode, DDR up to 400 MBps
- eMMC boot up mode
- Command Queue (CMDQ)
- Advanced Encryption Standard (AES)

The MSDC1 and MSDC2 controllers fully support:

- 32-bit data access on AHB bus
- 1-, 4-bit data bus width for SD card interface
- 1-, 4-bit data bus width for SDIO interface
- Default Speed mode, data rate up to 12.5 MBps
- High-speed mode, data rate up to 25 MBps
- SDR12 mode, data rate up to 12.5 MBps
- SDR25 mode, data rate up to 25 MBps
- SDR50 mode, data rate up to 50 MBps
- SDR104 mode, data rate up to 104 MBps
- DDR50 mode, data rate up to 50 MBps

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3.7.1.1 MSDC Signal Descriptions

Table 3-16 presents MSDC signal descriptions.

Table 3-16 MSDC signal descriptions

Signal name	Type	Description	Ball location
MSDC0			
MSDC0_CLK	DO	eMMC clock output	F32
MSDC0_CMD	DIO	eMMC command	F33
MSDC0_DAT0	DIO	eMMC data 0	D33
MSDC0_DAT1	DIO	eMMC data 1	F36
MSDC0_DAT2	DIO	eMMC data 2	D36
MSDC0_DAT3	DIO	eMMC data 3	E32
MSDC0_DAT4	DIO	eMMC data 4	D35
MSDC0_DAT5	DIO	eMMC data 5	F37
MSDC0_DAT6	DIO	eMMC data 6	E36
MSDC0_DAT7	DIO	eMMC data 7	D37
MSDC0_DSL	DI	eMMC data strobe input	E35
MSDC0_RSTB	DO	eMMC reset output	E34
MSDC1			
MSDC1_CLK	DO	SD card clock output	D4
MSDC1_CMD	DIO	SD card command	D3
MSDC1_DAT0	DIO	SD card data 0	D2
MSDC1_DAT1	DIO	SD card data 1	D1
MSDC1_DAT2	DIO	SD card data 2	C4
MSDC1_DAT3	DIO	SD card data 3	C3
MSDC2			
MSDC2_CLK	DO	SD card / SDIO clock output	AD35
MSDC2_CMD	DIO	SD card / SDIO command	AC35
MSDC2_DAT0	DIO	SD card / SDIO data 0	AD37
MSDC2_DAT1	DIO	SD card / SDIO data 1	AD36
MSDC2_DAT2	DIO	SD card / SDIO data 2	AB37
MSDC2_DAT3	DIO	SD card / SDIO data 3	AB35

3.7.1.2 MSDC Signal Mapping

The communication protocol between controller and device is implemented through an advanced 11-signal or 6-signal bus. Details are provided in Table 3-17.

Table 3-17 MSDC signal mapping

No.	Name [3.7)(1)]	Type	eMMC	SD/SDHC	SDIO	Description
1	MSDC0/1/2_CLK	DO	CLK	CLK	SCLK	Clock
2	MSDC0_RSTB	DO	RST_n			Reset output
3	MSDC0/1/2_DAT0	DIO	DAT0	DAT0	DAT0	Serial data line bit 0
4	MSDC0/1/2_DAT1	DIO	DAT1	DAT1	DAT1	Serial data line bit1
5	MSDC0/1/2_DAT2	DIO	DAT2	DAT2	DAT2	Serial data line bit 2

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No.	Name [3.7][1]	Type	eMMC	SD/SDHC	SDIO	Description
6	MSDC0/1/2_DAT3	DIO	DAT3	DAT3	DAT3	Serial data line bit 3
7	MSDC0_DAT4	DIO	DAT4			Serial data line bit 4
8	MSDC0_DAT5	DIO	DAT5			Serial data line bit 5
9	MSDC0_DAT6	DIO	DAT6			Serial data line bit 6
10	MSDC0_DAT7	DIO	DAT7			Serial data line bit 7
11	MSDC0/1/2_CMD	DIO	CMD	CMD	BS	Command/bus state
12	SD_WP[2]	DI		WP		Write protection
13	SD_INS[2]	DI	VSS2	VSS2	INS	Card insertion

1. All embedded pull-up and pull-down resistors can be disabled by programming the corresponding control registers if optimal pull-up or pull-down resistors are required on the system board.
2. SD_WP and SD_INS signals are not provided by MSDC controller. These functions can be accomplished using GPIO pins, if needed.

3.7.1.3 MSDC Timing Characteristics

Table 3-18 and Figure 3-11 present the MSDC timing characteristics in Default Speed mode.

Table 3-18 MSDC timing characteristics (default speed mode)

No.	Symbol	Parameter	Min.	Max.	Unit
Clock CLK (CLK rise and fall times are measured by min V_{IH} and max V_{IL}); C_{CARD} ≤ 10 pF					
DS1	f_{OP}	Operating frequency data transfer mode	0	25	MHz
	f_{OP_ID}	Operating frequency identification mode	100	400	kHz
DS2	$t_{w\_CLK\_L}$	Pulse duration, CLK low	10		ns
DS3	$t_{w\_CLK\_H}$	Pulse duration, CLK high	10		ns
DS4	t_{RISE_CLK}	Rise time, CLK		10	ns
DS5	t_{FALL_CLK}	Fall time, CLK		10	ns
Input DAT/CMD (referenced to CLK); C_{CARD} ≤ 10 pF					
DS6	$t_{su\_DAT/CMD}$	Setup time, DAT/CMD input	5		ns
DS7	$t_{h\_DAT/CMD}$	Hold time, DAT/CMD input	5		ns
Output DAT/CMD (referenced to CLK); C_L ≤ 40 pF					
DS8	$t_{d\_DAT/CMD}$	Delay time, DAT/CMD output during data transfer mode	0	14	ns
DS9	t_{d_DAT/CMD_ID}	Delay time, DAT/CMD output during identification mode	0	50	ns

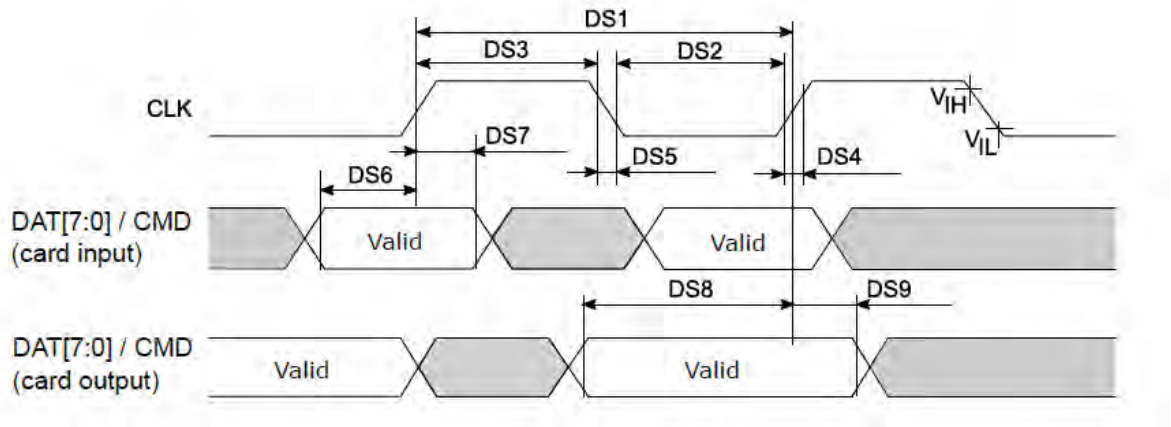

Figure 3-11 MSDC timing diagram (default speed mode)

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Table 3-19 and Table 3-12 present the MSDC timing characteristics in High Speed mode.

Table 3-19 MSDC timing characteristics (high speed mode)

No.	Symbol	Parameter		Min.	Max.	Unit
Clock CLK (CLK rise and fall times are measured by min V_{IH} and max V_{IL}); C_{CARD} ≤ 10 pF						
HS1	f_{OP}	Operating frequency data transfer mode		0	50	MHz
HS2	$t_{w\_CLK\_L}$	Pulse duration, CLK low		7		ns
HS3	$t_{w\_CLK\_H}$	Pulse duration, CLK high		7		ns
HS4	t_{RISE_CLK}	Rise time, CLK			3	ns
HS5	t_{FALL_CLK}	Fall time, CLK			3	ns
Input DAT/CMD (referenced to CLK); C_{CARD} ≤ 10 pF						
HS6	$t_{su\_DAT/CMD}$	Setup time, DAT/CMD input		6		ns
HS7	$t_{h\_DAT/CMD}$	Hold time, DAT/CMD input		2		ns
Output DAT/CMD (referenced to CLK)						
HS8	$t_{d\_DAT/CMD}$	Delay time, DAT/CMD output(1)	C_L ≤ 40 pF		14	ns
HS9	t_{d_DAT/CMD_ID}	Delay time, DAT/CMD output(1)	C_L ≤ 50 pF	2.5		ns
	C_L	Total system capacitance for each line			40	pF

1. Valid during data transfer mode.

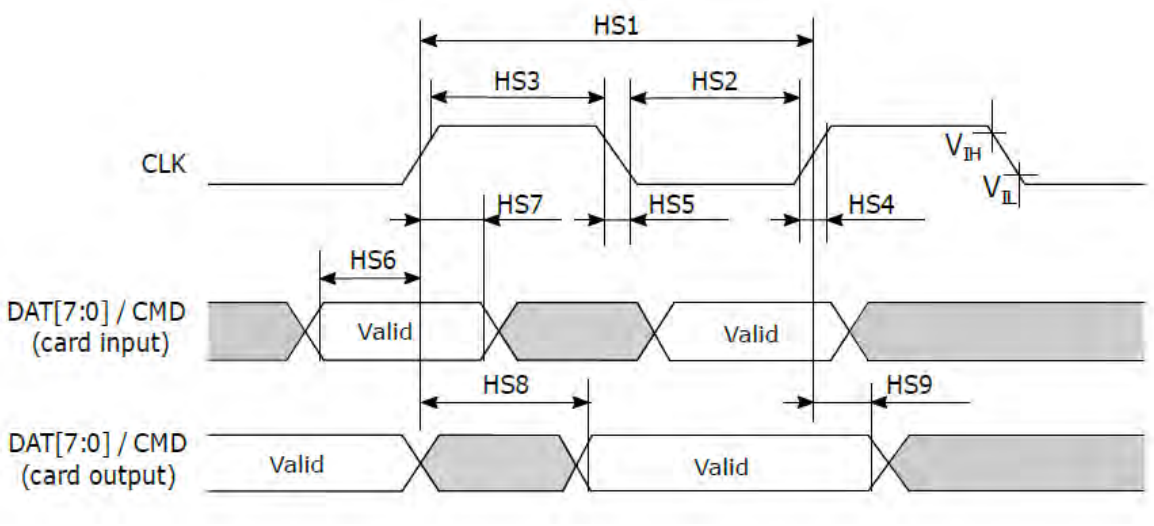

Figure 3-12 MSDC timing diagram (high speed mode)

Table 3-20 and Figure 3-13 present the MSDC timing characteristics in SDR12, SDR25, SDR50, and SDR104 modes.

Table 3-20 MSDC timing characteristics (SDR12/SDR25/SDR50/SDR104 modes)

No.	Symbol	Parameter	Min.	Max.	Unit
CLK output from host					
SDR121	t_C	Cycle time, CLK for SDR12		40	ns
		Cycle time, CLK for SDR25		20	ns
		Cycle time, CLK for SDR50		10	ns
		Cycle time, CLK for SDR104		4.8(4)	ns
SDR122	$t_{w\_CLK\_L}$	Pulse duration, CLK low for SDR25	10		ns
		Pulse duration, CLK low for SDR50	6.5		ns

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No.	Symbol	Parameter	Min.	Max.	Unit
SDR123	$t_{w\_CLK\_H}$	Pulse duration, CLK high for SDR25	10		ns
		Pulse duration, CLK high for SDR50	6.5		ns
	D	Duty Cycle, CLK	30	70	%
SDR124	t_{RISE_CLK}	Rise time, CLK		0.2 × SDR121[1]	ns
SDR125	t_{FALL_CLK}	Fall time, CLK		0.2 × SDR121[1]	ns
Host DAT/CMD input (referenced to CLK), V_{CT} = 0.975 V					
SDR126	$t_{su\_DAT/CMD}$	Setup time, DAT/CMD input for SDR50, C_{CARD} =10 pF	3		ns
		Setup time, DAT/CMD input for SDR104, C_{CARD} =10 pF	1.4		ns
SDR127	$t_{h\_DAT/CMD}$	Hold time, DAT/CMD input for SDR50, C_{CARD} = 5pF	0.8		ns
		Hold time, DAT/CMD input for SDR104, C_{CARD} = 5pF	0.8		ns
Host DAT/CMD output (referenced to CLK)					
SDR128	$t_{d\_DAT/CMD}$	Delay time, DAT/CMD output for SDR12/SDR25, $t_C \geq 20.0$ ns, C_L = 40 pF, using driver type B		14	ns
		Delay time, DAT/CMD output for SDR50, $t_C \geq 10.0$ ns, C_L = 30 pF, using driver type B		7.5	ns
		Delay time, DAT/CMD output for SDR104	0	2	UI[2]
	$\Delta t_{d\_DAT/CMD}$	Delay variation due to temperature change after tuning for SDR104	-350	+1550	ns
SDR129	$t_{h\_DAT/CMD}$	Hold time, DAT/CMD output for SDR12/SDR25/SDR50, C_L = 15 pF	1.5		ps
SDR1210	$t_{h\_DAT/CMD}$	Hold time, DAT/CMD output for SDR104	0.6[3]		UI[2]

1. $t_{RISE\_CLK}/t_{FALL\_CLK}$ < 0.96 ns (max) at 208 MHz, C_{CARD} = 10 pF; $t_{RISE\_CLK}/t_{FALL\_CLK}$ < 2 ns (max) at 100 MHz, C_{CARD} = 10 pF. The absolute maximum value of t_{RISE_CLK} and t_{FALL_CLK} is 10 ns regardless of the clock frequency.
2. Unit Interval (UI) is one bit nominal time. For example, UI = 5 ns at 200 MHz.
3. $t_{h\_DAT/CMD}$ = 2.88 ns at 208 MHz
4. Maximum 208 MHz, V_{CT} = 0.975V

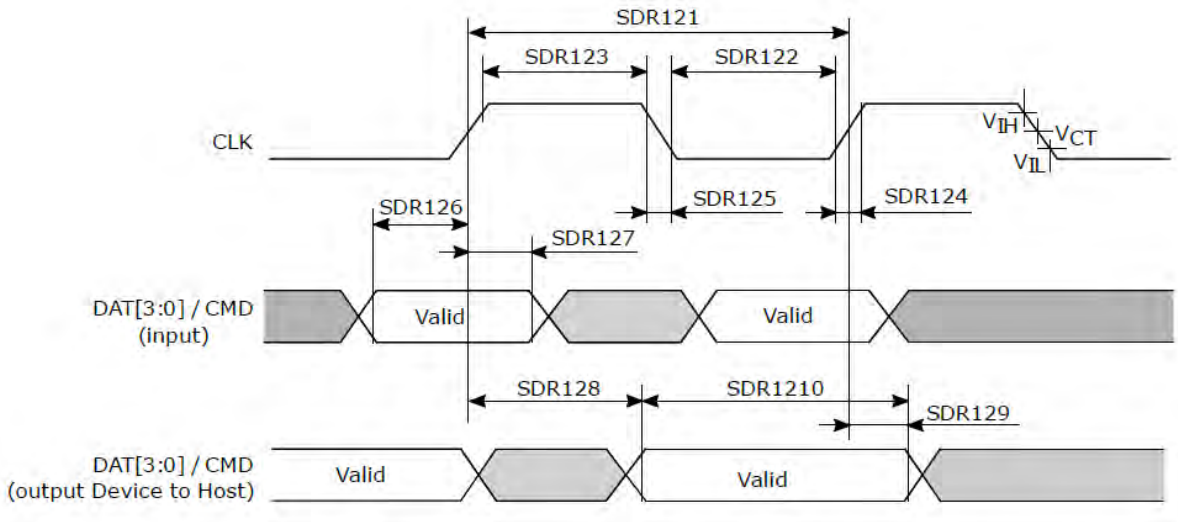

Figure 3-13 MSDC timing diagram (SDR12/SDR25/SDR50/SDR104 modes)

Table 3-21 and Figure 3-14 present the MSDC timing characteristics in DDR50 mode.

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Table 3-21 MSDC timing characteristics (DDR50 mode)

No.	Symbol	Parameter		Min.	Max.	Unit
Input DAT/CMD (referenced to CLK rising and falling edge/rising edge); C_{CARD} ≤ 10 pF						
DDR503	t_{su_CMD}	Setup time, CMD input		6		ns
	t_{su_DAT}	Setup time, DAT input		3		ns
DDR504	t_{h_CMD}	Hold time, CMD input		0.8		ns
	t_{h_DAT}	Hold time, DAT input		0.8		ns
Output DAT/CMD (referenced to CLK rising and falling edge/rising edge)						
DDR505	t_{d_CMD}	Delay time, CMD output(1)	C_L ≤ 30 pF		13.7	ns
	t_{d_DAT}	Delay time, DAT output(1)	C_L ≤ 25 pF		7	ns
DDR506	t_{h_CMD}	Hold time, CMD output	C_L ≤ 15 pF	1.5		ns
	t_{h_DAT}	Hold time, DAT output	C_L ≤ 15 pF	1.5		ns

1. Valid during data transfer mode.

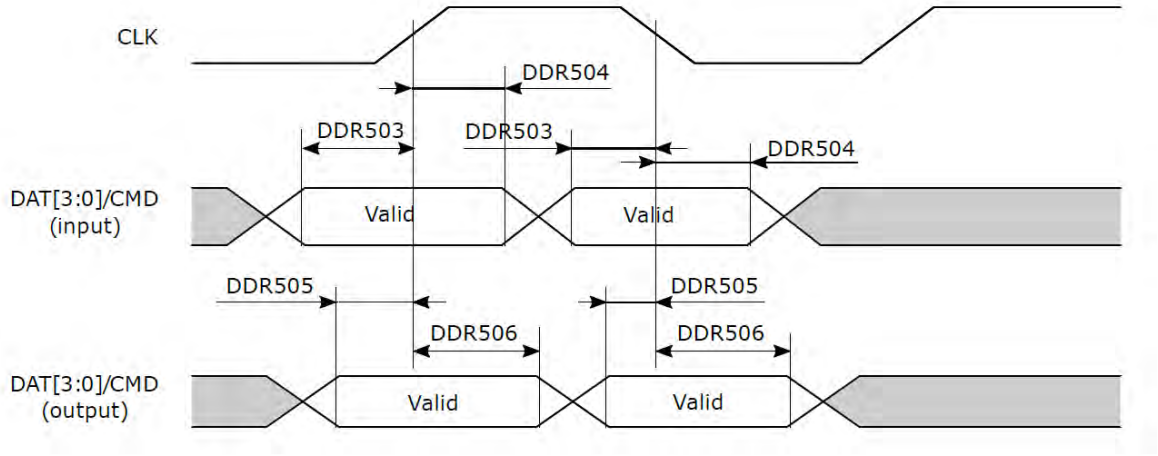

Figure 3-14 MSDC timing diagram (DDR50 mode)

Table 3-22 and Figure 3-15 present the MSDC timing characteristics in HS200 mode.

Table 3-22 MSDC timing characteristics (HS200 mode)

No.	Symbol	Parameter	Min.	Max.	Unit
Clock CLK					
HS2001	t_C	Cycle time, CLK	5		ns
HS2002	t_{RISE_CLK}	Rise time, CLK (C_{Device} ≤ 6 pF)		1(4)	ns
HS2003	t_{FALL_CLK}	Fall time, CLK (C_{Device} ≤ 6 pF)		1(4)	ns
	D	Duty Cycle, CLK	30	70	%
Input DAT/CMD; C_{Device} ≤ 6 pF					
HS2005	$t_{su\_DAT/CMD}$	Setup time, DAT/CMD input	1.4		ns
HS2006	$t_{h\_DAT/CMD}$	Hold time, DAT/CMD input	0.8		ns
Output DAT/CMD					
HS2007	$t_{d\_DAT/CMD}$	Delay time, DAT/CMD output	0	2	UI(1)
	$\Delta t_{d\_DAT/CMD}$	Delay variation due to temperature change after tuning(2)	-350 (ΔT=-20°C)	1550 (ΔT=90°C)	ps
HS2008	$t_{h\_DAT/CMD}$	Hold time, DAT/CMD output	0.575(3)		UI(1)

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1. Unit Interval (UI) is one bit nominal time. For example, UI = 5 ns at 200 MHz.
2. Total allowable shift of output valid window ($t_{h\_DAT/CMD}$) from last system tuning procedure $\Delta t_{d\_DAT/CMD}$ is 2600 ps for ΔT from -25 °C to 125 °C during operation.
3. The minimum value is equal to 2.88 ns at 208 MHz.
4. The absolute maximum value of t_{RISE_CLK} and t_{FALL_CLK} is 10 ns regardless of the clock frequency.

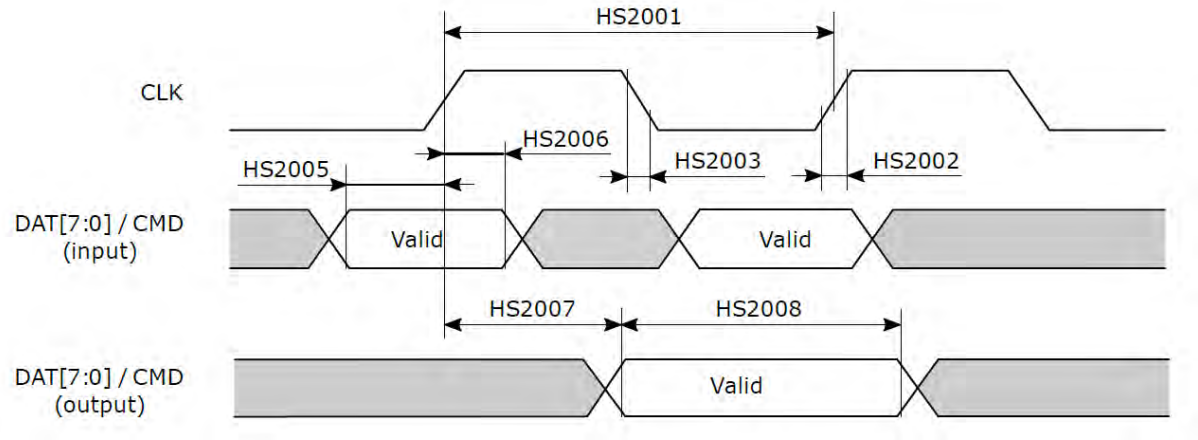

Figure 3-15 MSDC timing diagram (HS200 mode)

Table 3-23, Figure 3-16, and Figure 3-17 present the MSDC timing characteristics in HS400 mode.

Table 3-23 MSDC timing characteristics (HS400 mode)

No.	Symbol	Parameter	Min.	Max.	Unit
Input CLK					
HS4001	t_{C_CLK}	Cycle time, CLK (with respect to V_T)	5		ns
	SR	Slew rate, with respect to V_{IH}/V_{IL}	1.125		V/ns
HS4002	t_{ck_dd}	Duty cycle distortion(1)	0	0.3	ns
HS4003	t_{W_CLK}	Pulse duration, CLK (with respect to V_T)	2.2		ns
Input DAT (referenced to CLK); with respect to V_{IH}/V_{IL}; (C_{Device} ≤ 6 pF)					
HS4004	t_{su_DAT}	Setup time, DAT input	0.4		ns
HS4005	t_{h_DAT}	Hold time, DAT input	0.4		ns
	SR	Slew rate	1.125		V/ns
Data Strobe					
HS4006	t_{C_CLK}	Cycle time, CLK (with respect to V_T)	5		ns
	SR	Slew rate (with respect to V_{OH}/V_{OL} and HS400 reference load)	1.125		V/ns
HS4007	t_{ds_dd}	Duty cycle distortion(2)	0	0.2	ns
HS4008	t_{W_CLK}	Pulse duration, CLK (with respect to V_T)	2		ns
	t_{RPRE}	Read preamble	0.4		t_{C_CLK}
	t_{RPST}	Read post-amble	0.4		t_{C_CLK}
Input DAT (referenced to Data Strobe); with respect to V_{OH}/V_{OL} and HS400 reference load					
HS4009	t_{RQ}	Output skew		0.4	ns
HS4010	t_{RQH}	Output hold skew		0.4	ns
	SR	Slew rate	1.125		V/ns

1. Allowable deviation from an ideal 50% duty cycle. With respect to V_T. Includes jitter and phase noise.
2. Allowable deviation from the input CLK duty cycle distortion (t_{ck_dd}). With respect to V_T. Includes jitter and phase

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noise.

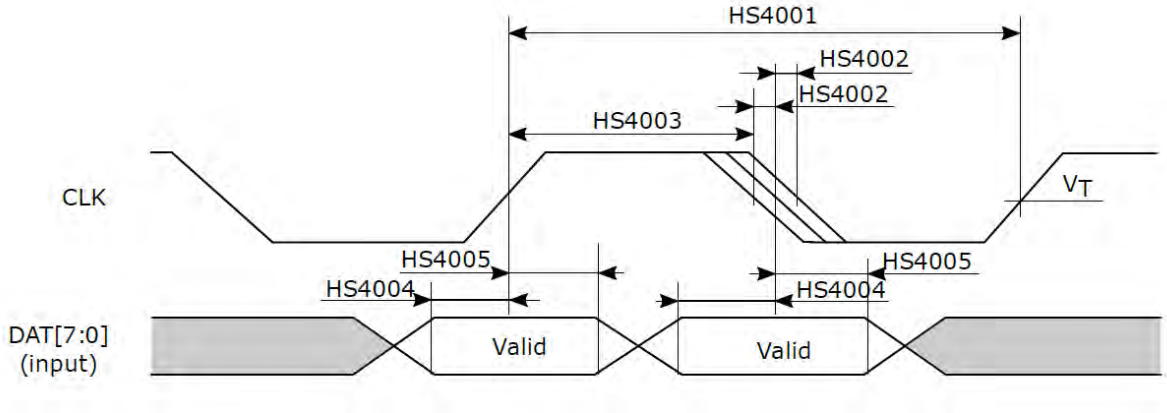

Figure 3-16 MSDC timing diagram (HS400 input mode)

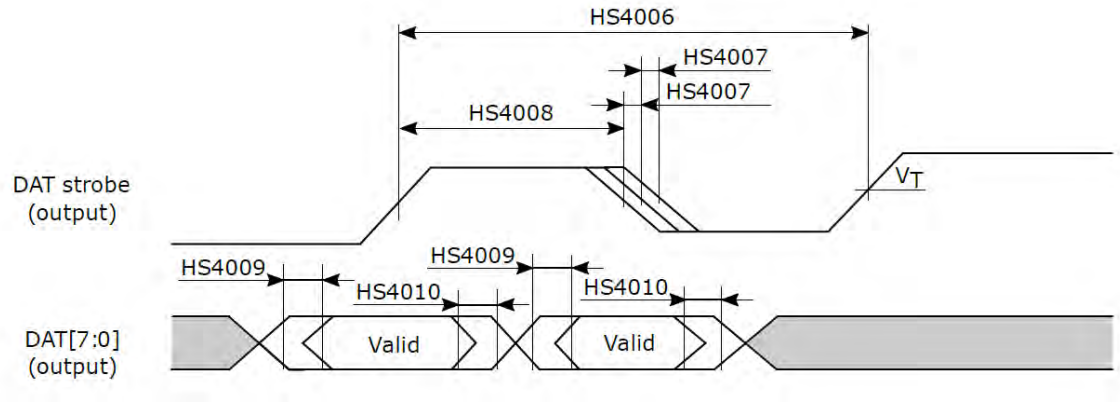

Figure 3-17 MSDC timing diagram (HS400 output mode)

3.7.2 Serial NOR (SNOR) Flash Interface

The device includes one Serial NOR (SNOR) Flash Interface controller.

The SNOR controller supports the following key features:

- SPI bus compatible serial interface for common serial NOR flash devices
- Maximum capacity of serial NOR flash device up to 512 Mbit
- 512-byte page programming buffer
- Multi-page program
- Single-bit SPI mode to transfer page program and 1-byte program
- 4-byte address mode and compatible 3-byte address mode
- Single-bit read mode
- Dual output and dual I/O read modes
- Quad output and quad I/O read modes
- The speed of SPI clock up to 52 MHz for single-bit SPI, dual-bit SPI and quad-bit SPI.
- Read of serial NOR flash data through Direct read mode, Programmed Input/Output (PIO) read mode, or DMA read mode

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3.7.2.1 SNOR Signal Descriptions

Table 3-24 presents SNOR signal descriptions.

Table 3-24 SNOR signal descriptions

Signal name	Type	Description	Ball location
SPINOR_CK	DO	SNOR clock	N30
SPINOR_CS	DO	SNOR chip select	N31
SPINOR_IO0	DIO	SNOR I/O data 0 (MOSI)	P30
SPINOR_IO1	DIO	SNOR I/O data 1 (MISO)	N34
SPINOR_IO2	DIO	SNOR I/O data 2 (WP)	P33
SPINOR_IO3	DIO	SNOR I/O data 3 (hold)	P35

3.7.2.2 SNOR Timing Characteristics

Table 3-25 and Figure 3-18 present the SNOR timing characteristics.

Table 3-25 SNOR timing characteristics

No.	Symbol	Parameter[1]	Min.	Max.	Unit
SNOR01	F_{ck}	SNOR clock (SF_SCLK) frequency		52	MHz
SNOR02	D	Duty Cycle, SF_SCLK	45	55	%
SNOR03	t_{CLQx}	Input setup time	5.776		ns
SNOR04	t_{CLQV}	Input hold time	−4.337		ns
SNOR05	t_d	Output delay		0.288	ns
SNOR06	t_h	Output hold time	−0.011		ns
SNOR07	$t_{R\_CS/SCLK}$	CS low to SF_SCLK rising edge (read)	1.5 / SCLK	9.5 / SCLK	ns
SNOR08	$t_{R\_SCLK/CS}$	SF_SCLK falling edge to CS high (read)	3 / SCLK	10 / SCLK	ns

1. The specification is based on the assumed load capacity value of 30 pF.

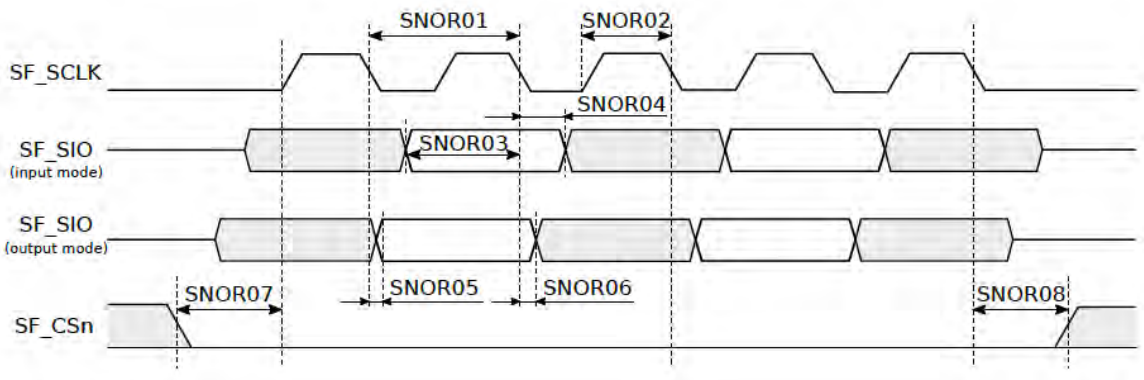

Figure 3-18 SNOR timing diagram

3.8 Display

The video data processing and display subsystem is also called Video data Processing Pipeline Subsystem (VPPSYS). It provides a variety of video data processing functions and display input/output interfaces. The video data processing functions can be served as video data post processing for Imaging or VDEC application, or as video data pre-processing for VENC, APU or Display application. The input data to VPPSYS can be channeled from DRAM buffer. The output data of

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VPPSYS can be channeled to DRAM buffer or to device display output interfaces. The device display output interfaces include MIPI DSI, eDP, DP and HDMI.

The Multimedia Data Path (MDP) inside VPPSYS is further divided into several categories:

- Video data processing pipelines: SVPP-0, SVPP-2 and SVPP-3 (see Section 3.8.1 Video Data Processing Pipelines (SVPP) and Interfaces)
- Display video data processing pipelines: DVPP-0 and DVPP-1 (see Section 3.8.2 Display Video Data Processing Pipelines (DVPP) and Interfaces)
- Image geometry warping engines: WPE (see Section 3.8.3 Warp Engine (WPE))

All the data processing pipes inside VPPSYS can be operated in either Standalone mode or In-line mode. In Standalone mode, the video data input come from DRAM buffer and the processed video data go to DRAM buffer as well. The start, stop and reset of the data processing in Standalone mode are fully controlled by software. In In-line mode, the data processing pipeline is directly connected with display input or output interfaces. In this mode, the start of video data processing is controlled by display interface timings. Software controls stop and reset of the data processing, and only updates the processing configuration when needed.
Both standalone and in-line modes are conducted through the Display MUTEX block (see Section 3.8.2.10 Display MUTEX (DISP_MUTEX)), which acts like an information dispatcher to all function blocks of VPPSYS about the start and stop of the video data processing.

3.8.1 Video Data Processing Pipelines (SVPP)

The SVPP-0 can operate standalone or in-line linked with the WPE engines. SVPP-2 and SVPP-3 can operate standalone.

The SVPP-0 pipeline provides the following features and corresponding functional blocks:

- Read DRAM agent: See Section 3.8.1.1 MDP Read DMA (MDP_RDMA)
- Image resizer and sharpness: See Section 3.8.1.5 MDP Resizer (MDP_RSZ) and Section 3.8.1.6 MDP 2D Sharpness Engine (MDP_TDSHP)
- Write DRAM agent with right angle (90-, 180-, 270-degree, left/right flip) image rotation: See Section 3.8.1.8 MDP Write Rotation DMA (MDP_WROT)
- Image aspect ratio converter: See Section 3.8.1.9 SVPP Padding (SVPP_PADDING)
- Maximum throughput of each SVPP: 420 Mpixel/s

The SVPP-2 and SVPP-3 pipelines provide the following features and corresponding functional blocks:

- Read DRAM agent: See Section 3.8.1.1 MDP Read DMA (MDP_RDMA)
- Fill grain noise for supporting AV1 spec: See Section 3.8.1.2 MDP Film Grain (MDP_FG)
- HDR transcode: See Section 3.8.1.3 MDP High Dynamic Range (MDP_HDR) Remapping
- Local contrast enhancement: See Section 3.8.1.4 MDP Adaptive Ambient Light Controller (MDP_AAL)
- Image resizer and sharpness: See Section 3.8.1.5 MDP Resizer (MDP_RSZ) and Section 3.8.1.6 MDP 2D Sharpness Engine (MDP_TDSHP)
- Preference color enhancement: See Section 3.8.1.7 MDP Color Engine (MDP_COLOR)
- Image aspect ratio converter: See Section 3.8.1.9 Video Processing Pipe Padding (VPP_PADDING)
- Write DRAM agent with right angle {90, 180, 270 degrees, left right flip} image rotation: See Section 3.8.1.8 MDP Write Rotation DMA (MDP_WROT)
- Maximum throughput of each SVPP: 420 Mpixel/s

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3.8.1.1 Multimedia Data Path Read DMA

The MDP_RDMA is a raster scan DMA used to access different input formats in memory. The MDP_RDMA reads data from memory, applies processing operations such as decode compression, block to raster, up-sampling, and color conversion, and outputs data in YUV444 or ARGB format to the next SVPP engine.

The MDP_RDMA provides the following main features:

- Multiple input image formats:
  - RGB (1 plane 8-bit)
  - ARGB (1 plane 8-bit/10-bit)
  - YUV444 (1 plane 8-bit/10-bit)
  - YUV422 (1 plane 8-bit, 2 planes 8-bit, 3 planes 8-bit)
  - YUV420 (2 planes 8-bit/10-bit, 3 planes 8-bit, 2 planes 8-bit/10-bit block mode)
  - Arm Frame Buffer Compression (AFBC) formats: YUV420 8-bit/10-bit, ARGB 8-bit/10-bit, Hybrid FBC YUV420 8-bit/10-bit)
- AFBC v1.1 support for the following configurations only:
  - 8-bit AFBC YUV420 (Layout1, no split, non-tiled)
  - AFBC_R8G8B8A8 (Layout3, split, non-tiled, no YUV transformation)
  - AFBC_R8G8B8A8 (Layout3, split, non-tiled, YUV transformation)
- Byte swap for switching input UV/RB data
- YUV444/ARGB/RGB output
- Clipping/cropping functions
- YUV420/422 chroma up-sampling filter to YUV444
- Color Space Conversion (CSC)
- AFBC and Hybrid FBC decompression into raster data

3.8.1.2 MDP Film Grain (MDP_FG)

The MDP_FG adds back film grain to the output video frames of the AV1 decoder.

The MDP_FG supports the following key features:

- AOMedia Video 1 (AV1) film grain
- 8-bit/10-bit mode
- Relay mode

3.8.1.3 MDP High Dynamic Range (MDP_HDR) Remapping

The MDP_HDR module processes HDR and wide-gamut signals, which can reach up to 10000 nits of dynamic range, to be displayed on a panel with much smaller dynamic range and gamut. The HDR remapped signals shown on a consumer display panel would look perceptually similar to the unprocessed signals shown on a HDR panel.

The MDP_HDR supports the following features:

- Electro-Optical Transfer Function (EOTF) options:
  - SMPTE ST 2084 (also called Perceptual Quantizer (PQ) or HDR10), providing a maximum of 4000 nits (2.5 times of PQ curve of 10000 nits) to better utilize the dynamic range of existing video streams.
  - British Broadcasting Corporation (BBC)/NHK Hybrid Log Gamma (HLG)
  - ITU-R BT.709

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  - SRGB
  - ITU-R BT.1886
- Optical-Electro Transfer Function (OETF) options:
  - ITU-R BT.709
  - BBC/NHK HLG
  - SMPTE ST 2084
  - SRGB
  - ITU-R BT.1886
- Programmable gamut
- YUV to RGB programmable color space conversion options:
  - Limited YCbCr BT.709 to full RGB
  - Limited YCbCr BT.2020 non-constant luminance to full RGB
  - Limited BT.2020 constant luminance to full RGB
- RGB to YUV programmable color space conversion:
  - Full RGB to limited YCbCr BT.709
- Adjustable tone-mapping curve (16 control points) and gain curve (1024 control points) to fine tune picture quality
- SMPTE ST 2086 static metadata and SMPTE ST 2094-40 dynamic metadata

3.8.1.4 MDP Adaptive Ambient Light Controller (MDP_AAL)

The MDP_AAL is coupled with the Smart Contrast Local Tone Mapping (SCLTM) and is used to improve picture quality by enhancing the contrast.

The MDP_AAL supports the following features:

- Color format: YUV
- 17-bin weighted histogram for each block
- 8 × 16 blocks for local contrast

3.8.1.5 MDP Resizer (MDP_RSZ)

The MDP_RSZ module is used to scale input image and video frames while preserving the signal energy at the same time.

The MDP_RSZ supports the following key features:

- Input/output data format: 10-bit YUV444
- Scaling ratio between 1/128× and 64×
- Up-scaling operation: 6-tap FIR (1 ≤ scaling ratio < 64)
- Down-scaling operations:
  - 4n-tap FIR (1/24 ≤ scaling ratio < 1)
  - Source accumulation (1/128 ≤ scaling ratio < 1/24)
- Fixed coefficients of the 6-tap and 4n-tap FIR filters

3.8.1.6 MDP 2D Sharpness Engine (MDP_TDSHP)

The sharpness function provides a better picture quality for display panels by restoring the image details, sharpening the edge and delivering a vivid feeling for pictures and videos.

The MDP_TDSHP supports the following features:

- Color format: YUV444

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- 2-dimensional sharpness filter
- Peaking by Color (PBC)
- Gain curve control
- Content analyzer

3.8.1.7 MDP Color Engine (MDP_COLOR)

The MDP_COLOR is a multi-stage processing engine used for achieving better picture quality and making one display panel resemble another in their output characteristics. It provides color space conversion functions and various hue/luma/saturation adjustments.

The COLOR supports the following key features:

- Color format: YUV444
- Input/output color space conversion
- C2P function: Transfer from Cartesian coordinates to Polar coordinates
- Hue engine functions:
  - Partial hue: Modifies hue angle of specific hue phase
- Y engine functions:
  - Partial Y: Modifies Y value of specific hue phase
  - Global contrast/brightness adjustment
  - Chroma boost: Compensates saturation value due to Y change
- Saturation engine functions:
  - Partial S: Modifies saturation value of specific hue phase
  - Saturation Gain by Y (SGainByY)
  - Global saturation adjustment
  - Low Saturation Protection (LSP) function for avoiding worsening side-effects of camera sensors, such as color shading protection.
- 3D color function for designing a color mapping window with adjustable location and size
- P2C function: Transfer from Polar coordinates to Cartesian coordinates

3.8.1.8 MDP Write Rotation DMA (MDP_WROT)

The MDP_WROT is a write-DMA agent with rotation and flip functions. It packs and transforms the input pixel-based data into 16 byte-wide output data.

The MDP_WROT provides the following key features:

- Rotation angles: 0°, 0° + H_Flip, 90°, 90° + H_Flip, 180°, 180° + H_Flip, 270°, and 270° + H_Flip
- Output image formats:
  - RGB888 (1 plane 8-bit), ARGB8888 (1 plane 8-bit/10-bit)
  - YUV444 (1 plane 8-bit/10-bit), YUV422 (1 plane 8-bit, 2 planes 8-bit, 3 planes 8-bit), YUV420 (2 planes 8-bit/10-bit, 3 planes 8-bit)
  - Compression format (AFBC YUV420 8-bit/10-bit, AFBC ARGB 8-bit/10-bit)
- AFBC v1.1 support for the following configurations only:
  - 8-bit AFBC YUV 4:2:0 (Layout1, no split, non-tiled)
  - AFBC_R8G8B8A8 (Layout3, split, non-tiled, no YUV transformation)
  - AFBC_R8G8B8A8 (Layout3, split, non-tiled, YUV transformation)

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- Byte swap for switching output UV/RB data
- Cropping function
- Color Space Conversion (CSC)
- YUV down-sample for output format YUV420 or YUV422

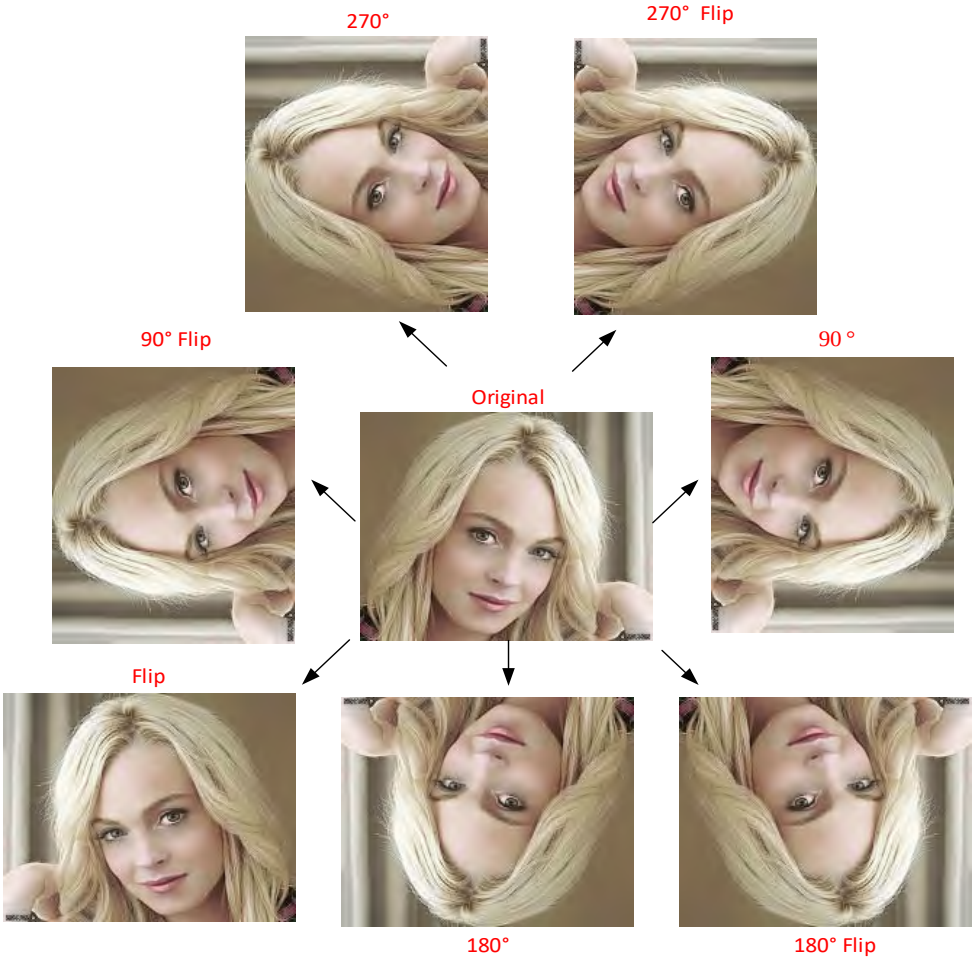

Figure 3-19 Eight rotation angles

3.8.1.9 Display Resizer (DISP_RSZ)

The DISP_RSZ module is used to scale input image.

The DISP_RSZ supports the following key features:

- Input/output data format: ARGB10101010
- Scaling ratio between 1× and 64×
- Support up-scaling operation
- Support 4-tap FIR

3.8.1.10 SVPP Padding (SVPP_PADDING)

The SVPP_PADDING module adjusts the aspect ratio of image source for different kinds of display panels.

The SVPP_PADDING supports the following features:

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- RGB101010 and 8-bit alpha formats
- Padding of the pre-defined color for configurable top/down/left/right side distance

3.8.2 Display Video Data Processing Pipelines (DVPP) and Interfaces

The DVPP-0 pipeline provides image blending and display image enhancement for on-device display through MIPI DSI and eDP interfaces. DVPP-1 provides image blending and High Dynamic Range (HDR) format conversion for external display connection through DP and HDMI interfaces.

The DVPP-0 pipeline provides the following features and corresponding functional blocks:

- Multi-layer image blender with wide color gamut support (self-equipped with read DRAM agent): See Section 3.8.2.1 Display Overlay (DISP_OVL)
- Preference color enhancement: See Section 3.8.2.2 Display Color Engine (DISP_COLOR)
- Display image tuning for on-device panel, including Color Space Conversion (CSC), global contrast, gamma, postmask and dither functions:
  - See Section 3.8.2.5 Display Color Correction (DISP_CCORR)
  - See Section 3.8.2.6 Display Adaptive Ambient Light Controller (DISP_AAL)
  - See Section 3.8.2.7 Display Gamma Engine (DISP_GAMMA)
  - See Section 3.8.2.8 Display Dither Engine (DISP_DITHER)
  - See Section 3.8.2.16 Display POSTMASK (DISP_POSTMASK)
- Data pipeline merger: See Section 3.8.2.9 Display Video Data Processing Pipeline Merger (DVPP_MERGE)
- MIPI Display Stream Compression (DSC): See Section 3.8.2.10 Display Stream Compression (DSC) Engine
- MIPI DSI controller: See Section 3.8.2.13 Display Serial Interface (DSI)
- eDP interface: See Section 3.8.4 Embedded DisplayPort Interface (EDPTX)
- Video data interface to EDPTX
- Maximum pixel throughput: 4K @ 30 Hz (297 Mpixel/sec)

The DVPP-1 pipeline provides the following features and corresponding functional blocks:

- HDR block supports external display with HDR10+: See Section 3.8.2.11.1 High Dynamic Range (HDR) Engine. Four read DRAM agents to support 4× HDR image layers
- Data pipeline merger: See Section 3.8.2.3 Display Video Data Processing Pipeline Merger (DVPP_MERGE)
- Digital video output: See Section 3.8.2.6 Display Digital Parallel Interface (DPI)
- DP interface: See Section 3.8.3 DisplayPort Interface (DPTX)
- Video data interface to DPTX, HDMITX
- Maximum pixel throughput: 4K @ 60 Hz (594 Mpixel/sec)

3.8.2.1 Display Overlay (DISP_OVL)

The DISP_OVL provides four flexible layers to implement alpha blending. The size, placement, format, and source of each layer can be configured independently. Data can be sourced from DRAM or directly from an upstream module in the display path.

The DISP_OVL supports the following key features:

- Four-layer alpha blending
- Maximum layer width:
  - 8191 pixels for data sourced from direct-link module or DRAM uncompressed data

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  - 3840 pixels for DRAM AFBC compressed data
- Maximum layer height:
  - 8191 pixels for data sourced from direct-link module or DRAM uncompressed data
  - 8184 pixels for DRAM AFBC compressed data
- DRAM uncompressed input color format:
  - ARGB2101010/ARGB8888/ARGB1555/RGB888
  - YUV444 (10bit, 1-plane)/YUV444 (8bit, 1-plane)
- DRAM AFBC v1.1 compressed input color formats:
  - AFBC_R10G10B10A2 (Layout 3, split, non-tiled, no YUV transform)
  - AFBC_R10G10B10A2 (Layout 3, split, non-tiled, YUV transform)
  - AFBC_R8G8B8A8 (Layout 3, split, non-tiled, no YUV transform)
  - AFBC_R8G8B8A8 (Layout 3, split, non-tiled, YUV transform)
  - AFBC_R8G8B8 (Layout 3, split, non-tiled, no YUV transform)
  - AFBC_R8G8B8 (Layout 3, split, non-tiled, YUV transform)
- YUV to RGB, and RGB to RGB color space conversion options with custom coefficients
- Gamma conversion and inverse gamma conversion for each layer
- Support RGB-to-RGB color conversion and gamma conversion for the merged layer
- Dynamic Clock Management (DCM) for power consumption reduction

The register OVL_[LAYER]_SRC_SIZE.[LAYER]_SRC_W must be a multiple of 32.
The register OVL_[LAYER]_SRC_SIZE.[LAYER]_SRC_H must be a multiple of 4.
The register OVL_[LAYER]_HDR_PITCH.[LAYER]_HDR_SRC_PITCH must be a multiple of 16.
The register OVL_[LAYER]_PITCH.[LAYER]_SRC_PITCH must be a multiple of “superblock size x bytes per pixel”.
The register OVL_[LAYER]_CLIP is used to adjust the output size of the layer for the size limitation of AFBC format. The proper clipping range should be "left clip < 32, right clip < 32, top clip < 4, and bottom clip < 4".
([LAYER] = L0 ~ L3)

3.8.2.2 Display Color Engine (DISP_COLOR)

The DISP_COLOR is a multi-stage processing engine used for achieving better picture quality and making one display panel resemble another in their output characteristics. It provides color space conversion functions and various hue/luma/saturation adjustments.

The DISP_COLOR supports the following key features:

- Color format: RGB
- Input/output color space conversion
- C2P function: Transfer from Cartesian coordinates to Polar coordinates
- Hue engine functions:
  - Partial hue: Modifies hue angle of specific hue phase
- Y engine:
  - Partial Y: Modifies Y value of specific hue phase
  - Global contrast/brightness adjustment
  - Chroma boost: Compensates saturation value due to Y change
- Saturation engine functions:
  - Partial S: Modifies saturation value of specific hue phase

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  - Saturation Gain by Y (SGainByY)
  - Global saturation adjustment
  - Low Saturation Protection (LSP) for avoiding worsening side-effects of camera sensors, such as color shading protection
- 3D color function for designing a color mapping window with adjustable location and size
- P2C function: Transfer from Polar coordinates to Cartesian coordinates

3.8.2.3 Display Read DMA (DISP_RDMA)

The DISP_RDMA engine reads out the data in the display pipeline from DRAM. The DISP_RDMA can also serve as a buffer for direct link data transfers from upstream modules.

The DISP_RDMA supports the following key features:

- Direct link input mode (DISP_RDMA receives data from upstream module and serves as a buffer)
  - Input color formats: RGB888, RGB101010
  - Output color formats: RGB888, RGB101010
- Memory input mode (DISP_RDMA reads data from DRAM and provides buffering)
  - Input color formats
    - YUYV422 (UYVY 8-bit, YUY2 8-bit, UYVY 10-bit, YUY2 10-bit)
    - RGB565, RGB888, ARGB4444, ARGB8888, ARGB2101010
    - Android_UYVY_10b, Android_YUY2_10b
  - Output color formats: RGB888, RGB101010
- Swapping and cropping functions
- Programmable Color Space Conversion (CSC)
- Maximum resolution and data depth: 3840 × 2160, 10-bit
- Universal Frame Buffer Compression (UFO) decoding for RGB888 and RGB101010 data

3.8.2.4 Display Write DMA (DISP_WDMA)

The DISP_WDMA writes out the data in the display pipeline into DRAM.

The DISP_WDMA provides the following key features:

- Input color formats: YUV444/RGB888/ARGB8888/ARGB2101010
- Output color formats:
  - YUV422 (UYVY, YUY2)/YUV420 (YV12, NV12, P010)/Y8
  - RGB565/RGB888/ARGB8888/ARGB2101010
- UFO encoding for RGB888 and RGB101010 data
- Programmable CSC
- 3-tap filter in horizontal direction and 2-tap filter in vertical direction for YUV444 down-sampling
- Swapping and clipping functions
- Maximum supported resolution: 3840 × 2160

3.8.2.5 Display Color Correction (DISP_CCORR)

The DISP_CCORR engine changes the overall mixture of RGB colors to fit the characteristics of the target display panel.

The DISP_CCORR supports the following key features:

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- Fixed-coefficient inverse gamma table (conversion of non-linear sRGB data to linear RGB data)
- Fixed-coefficient gamma table (conversion of linear RGB data back to non-linear sRGB data)
  (Gamut mapping should be in linear domain).
- Programmable 3 × 3 matrix and color offset

3.8.2.6 Display Adaptive Ambient Light Controller (DISP_AAL)

The DSIP_AAL controller provides content adaptive and ambient light adaptive functions. It is responsible for backlight power saving and sunlight visibility improvement.

The DISP_AAL provides the following key features:

- Supported input color format: RGB
- 33-bin weighted histogram
- Dark Region Enhancement (DRE) mapping for sunlight visibility
- Content Adaptive Backlight Control (CABC) compensation for backlight power saving

3.8.2.7 Display GAMMA Engine (DISP_GAMMA)

The DISP_GAMMA engine provides gamma correction by changing the overall mixture of RGB colors to fit the characteristics of the display panel.

The DISP_GAMMA supports the following key features:

- 10-bit gamma table with 1024 entries
- Non-block gamma LUT programming

3.8.2.8 Display Dither Engine (DISP_DITHER)

The DISP_DITHER is used to decrease the RGB depth while mitigating the loss of quality at the same time.

3.8.2.9 Display Video Data Processing Pipeline Merger (DVPP_MERGE)

The VPP_MERGE module is used to merge two slice-per-line inputs into one side-by-side output. The device includes two VPP_MERGE modules, VPP_MERGE0 and VPP_MERG1.
Each VPP_MERGE module supports the following features:

- Input color formats and ranges:
  - Input 0: ARGB/AYCbCr444/YCbCr422; 8-bit Alpha, 10-bit color, full range
  - Input 1: ARGB/AYCbCr444; 8-bit Alpha, 10-bit color, full range
- Output color formats and ranges:
  - Output 0: ARGB/AYCbCr444; 8-bit Alpha, 12-bit color, full range
  - Output 1: ARGB/AYCbCr444; 8-bit Alpha, 10-bit color, full range
- Input/output RGB/YUV channel swap
- Split input into two slice-per-line outputs
- YCbCr422 to YCbCr444 up-sampling
- Color range extension from 10-bit to 12-bit

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3.8.2.10 Display Stream Compression (DSC) Engine

The DSC engine is a video data compressor. Data compression allows less data transmission for the purpose of achieving power saving and high video frame rate.

The DSC engine contains two processing cores, which perform the data compression.

- Compliance with VESA DSC1.2a
- 8-bit/10-bit RGB data formats
- Maximum horizontal slices: 2
- Maximum slice width: 1920 pixels
- Rate Control (RC) buffer size: 32955-bit
- Maximum line buffer bit depth: 11-bit
- Block prediction function

3.8.2.11 Display Video Data Output High Dynamic Range (VDO_HDR)

The VDO_HDR block provides HDR10+ function for external displays.

3.8.2.11.1 High Dynamic Range (HDR) Engine

The HDR engine converts a Standard Dynamic Range (SDR) or HDR-encoded stream into panel-displayable content, which can be SDR or HDR format.

The HDR engine supports the following key features:

- Video stream properties: 4K YCbCr 4:4:4 10-bit
- Color space conversion between RGB and YCbCr
- SDR (gamma 2.2)
- HDR10, Hybrid Log-Gamma, and HDR10+
- Tone-Mapping when converting HDR into SDR, with content maximally preserved
- Tone-Mapping when converting SDR into HDR, with optimized visual effect
- Compliance with BT. 2100 standard
- Compliance with HDR10+ technical specification

3.8.2.11.2 Display Mixer (DISP_MIXER)

The DISP_MIXER performs alpha blending of up to four layers of HDR display content. Two layers are sourced from the main video and sub-video data paths, while the other two layers are sourced from the Ultra High Definition On-Screen Display (UHD OSD) and Full High-Definition On-Screen Display (FHD OSD) graphics paths.

The DISP_MIXER supports the following main features:

- Video frame resolution: Up to 4096 × 2160
- Pre-multiplied and non-pre-multiplied alpha blending
- Pixel alpha blending
- Flexible Region of Interest (ROI)

3.8.2.11.2.1 Block Diagram

Figure 3-20 illustrates the architecture of DISP_MIXER, and the function of each module is described as follows.

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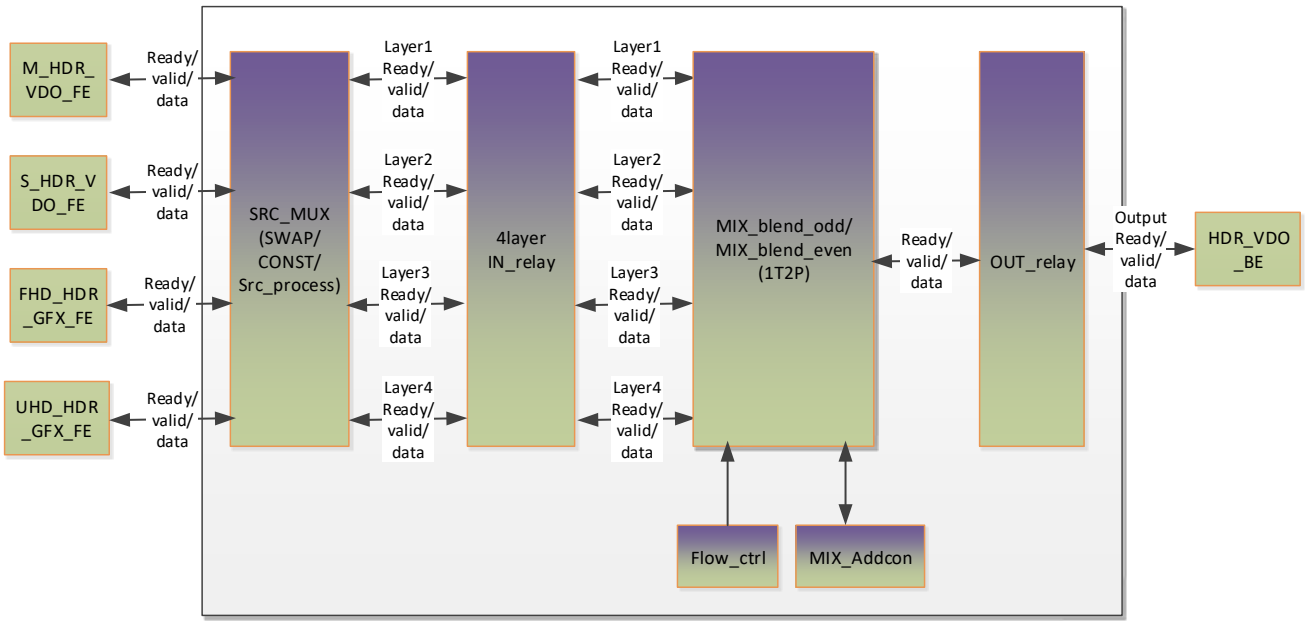

Figure 3-20 Block diagram of DISP_MIXER

After SRC_MUX, four layers go through IN_relay module separately, then execute blending function at MIX_blend_odd/MIX_blend_even module, and finally are output to the next module after passing OUT_relay module.

- SRC_MUX:
  - Four layers can be swapped at this module.
  - Each layer can be replaced by constant.
- MIX_blend_odd/MIX_blend_even: Perform alpha blending.
- Flow_ctrl: Control the workflow of DISP_MIXER.
- MIX_Addcon: Calculate the pixel coordination and region position of each layer.

3.8.2.11.2.2 Theory of Operations

The formula of the alpha blending is selected by source color format automatically. The variables used in the following equations are illustrated in the following description:

- src.r, src.g, src.b and src.a are this layer's pixel value and alpha.
- dst.r, dst.g, dst.b and dst.a are the results of alpha blending of all lower layers.
- DST.r, DST.g, DST.b are the results of alpha blending of the current layer.
- If source color format is ARGB888 8-bit, then the alpha blending formula is
  DST.r = (dst.r *(255-alpha) + alpha*src.r + (dst.r*(255-alpha) + alpha*src.r)>>8 + 128)>>8.
  DST.g = (dst.g*(255-alpha) + alpha*src.g + (dst.g*(255-alpha) + alpha*src.g)>>8 + 128)>>8.
  DST.b = (dst.b*(255-alpha) + alpha*src.b + (dst.b*(255-alpha) + alpha*src.b)>>8 + 128)>>8.

3.8.2.12 Display Digital Parallel Interface (DPI)

The device includes two DPI controllers, DPI0 and DPI1, which output digital video data and timing signals. DPI0 is used to directly interface an external display panel, while DPI1 provides data and timings to HDMITX module.

Each DPI controller supports the following key features:

- Flexible output data bus width and formats:

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- DPI0 up to 16-bit bus: RGB565/YUV422 8-bit
- DPI1 up to 30-bit bus: RGB565/RGB 8-bit, 10-bit/YUV444 8-bit, 10-bit/YUV422 8-bit, 10-bit, 12-bit
- Resolution up to 1920 × 1080 @ 60fps (for DPI0 only)
- Color space conversion
- Embedded synchronization timings for BT.656-like output format
- Dual edge output format
- YUV444 to YUV422 chroma down-sampling
- Internal pattern generator

3.8.2.12.1 DPI Signal Descriptions

Table 3-26 presents DPI signal descriptions.

Table 3-26 DPI signal descriptions

Signal name	Type	Description	Ball location
DPI_CK	DO	DPI pixel clock	AB1
DPI_D0	DO	DPI data 0	AB9
DPI_D1	DO	DPI data 1	AC9
DPI_D10	DO	DPI data 10	AC5
DPI_D11	DO	DPI data 11	AA5
DPI_D12	DO	DPI data 12	AA6
DPI_D13	DO	DPI data 13	AC6
DPI_D14	DO	DPI data 14	AC7
DPI_D15	DO	DPI data 15	AB4
DPI_D2	DO	DPI data 2	AB8
DPI_D3	DO	DPI data 3	AC4
DPI_D4	DO	DPI data 4	AB3
DPI_D5	DO	DPI data 5	AA8
DPI_D6	DO	DPI data 6	AC8
DPI_D7	DO	DPI data 7	AB7
DPI_D8	DO	DPI data 8	AB6
DPI_D9	DO	DPI data 9	AB5
DPI_DE	DO	DPI data enable	AB2
DPI_HSYNC	DO	DPI horizontal synchronization	AD11
DPI_VSYNC	DO	DPI vertical synchronization	AD10

3.8.2.12.2 DPI Timing Characteristics

Table 3-27 and Figure 3-21 present timing characteristics for DPI in the device.

Table 3-27 DPI timing characteristics

No.	Parameter		Min.	Max.	Unit
DPI01	t_C	Cycle time	6.73[1]		ns
DPI02	D	Duty cycle, DPI_CK	45	55	%
DPI03	t_{RISE}	Rise time		t_c /5	ns
DPI04	t_{FALL}	Fall time		t_c /5	ns

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No.	Parameter		Min.	Max.	Unit
DPI05	t_d	Delay time, other signals to DPI_CK	t_c /4		ns

1. For maximum operating clock frequency refer to Table 6-1 Maximum performance ratings.

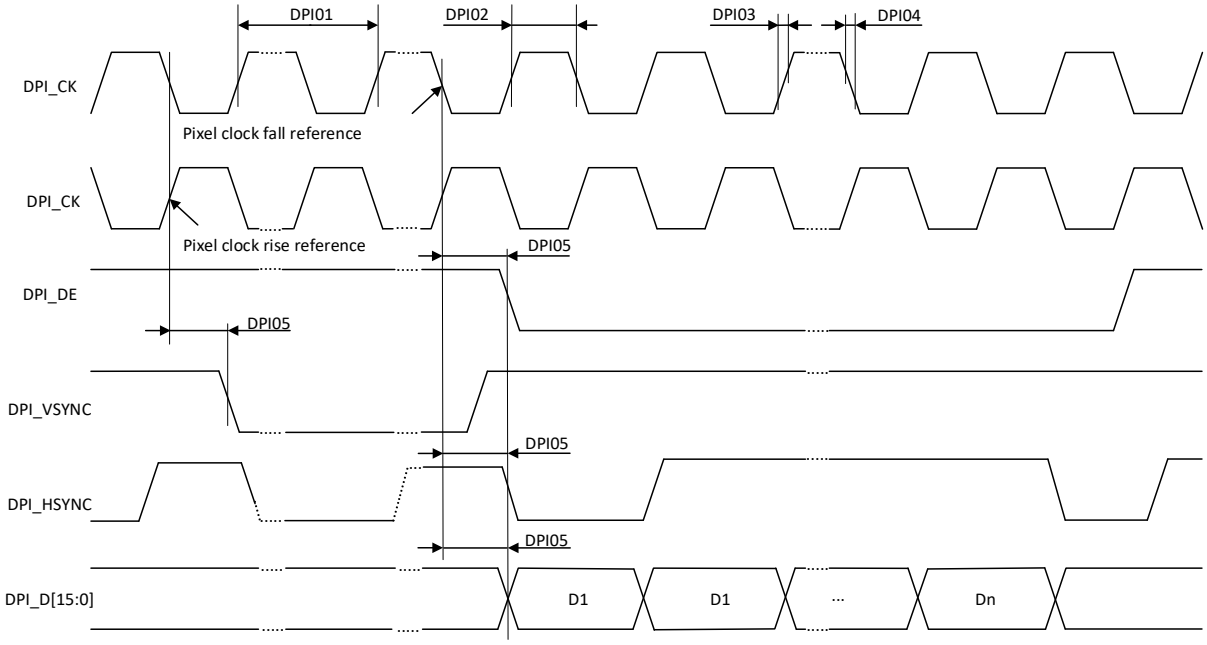

Figure 3-21 DPI timing diagram

3.8.2.13 Display Serial Interface (DSI)

The DSI is based on MIPI Alliance Specification, supporting high-speed serial data transfer between host processor and peripheral devices such as display modules.

The device includes two DSI controllers, DSI0 and DSI1. Each DSI controller receives frame pixels from memory, performs frames packing and lane distribution, and then sends the data to a dedicated MIPI D-PHY/C-PHY TX core for serializing.

Each DSI controller provides the following key features:

- Compliance with MIPI DSI Specification DSI-2 v1.0
- Supports video and command mode data transfers
- Pixel format of RGB888/RGB101010/compressed pixel stream
- 128-enrty command queue for command transmission
- 3 types of video modes: sync-event, sync-pulse, burst modes
- Limited high-speed residual packet transmission during video mode blanking period
- Ultra-low power mode control
- Peripheral and external Tearing Effect (TE) signal detection
- MIPI D-PHY interface, with the following features:
  - 1 clock lane and up to 4 data lanes
  - Throughput up to 1.2 Gbps per data lane
  - Bidirectional data transmission in Low-Power mode for data lane 0
  - Uni-directional data transmission in High-Speed mode for data lanes 0 through 3
  - Non-continuous high-speed transmission for clock and data lanes

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  - Lane swapping
  - Compliance with MIPI D-PHY Specification v1.2
- MIPI CPHY interface, with the following features:
  - Single 3-trio port
  - Throughput up to 1.1 Gsps per trio
  - Trio swapping
  - Compliance with MIPI C-PHY Specification v1.0
- Each D-PHY/C-PHY TX core provides the following main features:
  - Sigma-Delta Modulation (SDM) PLL configuration
  - Spread Spectrum Clocking (SSC) control
  - Bandgap control
  - Output pads control

3.8.2.13.1 DSI Signal Descriptions

Table 3-28 presents DSI signal descriptions.

Table 3-28 DSI signal descriptions

Signal name	Type	Description		Ball location
DSI1		**D-PHY Mode**	**C-PHY Mode**	
DSI1_CKN_T1C	AIO	DSI1 clock lane (negative)	DSI1 Trio1 C	AK6
DSI1_CKP_T1B	AIO	DSI1 clock lane (positive)	DSI1 Trio1 B	AK7
DSI1_D0N_T1A	AIO	DSI1 data lane 0 (negative)	DSI1 Trio1 A	AK5
DSI1_D0P_T0C	AIO	DSI1 data lane 0 (positive)	DSI1 Trio0 C	AL5
DSI1_D1N_T2B	AIO	DSI1 data lane 1 (negative)	DSI1 Trio2 B	AL6
DSI1_D1P_T2A	AIO	DSI1 data lane 1 (positive)	DSI1 Trio2 A	AL7
DSI1_D2N_T0B	AIO	DSI1 data lane 2 (negative)	DSI1 Trio0 B	AL4
DSI1_D2P_T0A	AIO	DSI1 data lane 2 (positive)	DSI1 Trio0 B	AL3
DSI1_D3N	AIO	DSI1 data lane 3 (negative)	-	AK8
DSI1_D3P_T2C	AIO	DSI1 data lane 3 (positive)	DSI1 Trio2 C	AL8
DSI1_TE	DI	DSI1 tearing effect control	DSI1 tearing effect control	Y5, AA7
DSI0		**D-PHY Mode**	**C-PHY Mode**	
DSI0_CKN_T1C	AIO	DSI0 clock lane (negative)	DSI0 Trio1 C	AH7
DSI0_CKP_T1B	AIO	DSI0 clock lane (positive)	DSI0 Trio1 B	AH6
DSI0_D0N_T1A	AIO	DSI0 data lane 0 (negative)	DSI0 Trio1 A	AH5
DSI0_D0P_T0C	AIO	DSI0 data lane 0 (positive)	DSI0 Trio0 C	AG5
DSI0_D1N_T2B	AIO	DSI0 data lane 1 (negative)	DSI0 Trio2 B	AH3
DSI0_D1P_T2A	AIO	DSI0 data lane 1 (positive)	DSI0 Trio2 A	AH4
DSI0_D2N_T0B	AIO	DSI0 data lane 2 (negative)	DSI0 Trio0 B	AG6
DSI0_D2P_T0A	AIO	DSI0 data lane 2 (positive)	DSI0 Trio0 A	AG7
DSI0_D3N	AIO	DSI0 data lane 3 (negative)	-	AH2
DSI0_D3P_T2C	AIO	DSI0 data lane 3 (positive)	DSI0 Trio2 C	AJ3
DSI_TE	DI	DSI0 tearing effect control	DSI0 tearing effect control	AA7, Y5

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3.8.2.13.2 DSI Timing Characteristics

The DSI interface timing and electrical characteristics are compliant with MIPI DSI Specification DSI-2 v1.0, MIPI D-PHY Specification v1.2, and MIPI C-PHY Specification v1.0.

3.8.2.14 Display MUTEX

The device supports multiple display paths. The DISP_MUTEX is used to synchronize the start trigger signal of each submodule in the display path. Each display path can be configured with different and independent timings, and multiple DISP_MUTEX cores are assigned to each path.

The DISP_MUTEX supports the following key features:

- Up to 16 MUTEX cores in parallel
- Each submodule in the display path can be assigned to any one of the MUTEX cores
- The start trigger signal for each MUTEX core is driven either from SW or from a display interface controller

The start trigger method determines the operation mode of the display path:

- Single mode (SW trigger):
  - Single frame processing upon every SW trigger
  - Memory in – memory out path
  - Memory in and directly link to command mode display output (for example, command mode)
- Refresh mode (display interface trigger):
  - Frame-by-frame processing after start
  - Memory in and direct link to video mode display output (for example, DSI video mode, DPI)

3.8.2.15 Display Pulse Width Modulation (DISP_PWM)

The DISP_PWM module provides PWM signals for the LED driver of an LCM in order to reduce its backlight power consumption.

The DISP_PWM supports the following features:

- Gradual PWM control
- Operating clocks: 16.25 MHz, 26 MHz, 65 MHz, 104 MHz or 130 MHz

3.8.2.15.1 DISP_PWM Signal Descriptions

Table 3-29 presents the DISP_PWM signal descriptions.

Table 3-29 DISP_PWM signal descriptions

Signal name	Type	Description	Ball location
DISP_PWM0	DO	Display PWM output 0	AA9, Y11
DISP_PWM1	DO	Display PWM output 1	AA9, Y11

3.8.2.16 Display POSTMASK Engine

The DISP_POSTMASK engine supports the rounded corner of image and the Notch of image.

The DISP_POSTMASK supports the following features:

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- SRAM mode: No DRAM access, simple rounded corner with limited gradient
- DRAM mode: Rounded corner and the maximum of 16 Notches
- Partial update

3.8.3 DisplayPort Interface (DPTX)

The DPTX provides digital video and auxiliary data transfer between the device and an external display module. The communication link is handled through the DP Auxiliary Channel (DPAUX).

The DPTX supports the following key features:

- Compliance with DP v1.4 standard
- Single link output port with 4× main lanes, configured as follows:
  - 4× lanes with up to 5.4 Gbps per lane (HBR3)
- Hot Plug Detect (HPD)
- Auxiliary channel lane:
  - Manchester-II coding
  - clock extracted from the data stream
  - 1 Mbps bit rate
- Input data formats: RGB 8-bit/10-bit, YUV444 8-bit/10-bit, YUV422 8-bit/10-bit
- Output data format: RGB444 8-bit/10-bit, YCbCr422 8-bit/10-bit
- 8-bit to 10-bit encoder
- Interlane skew function
- Up to 4K2K @ 60 Hz resolution (10-bit)
- Main functions:
  - HDCP13
  - HDCP22
  - FEC
  - DSC
  - HDR
  - Adaptive sync

3.8.3.1 DPTX Signal Descriptions

Table 3-30 presents DPTX signal descriptions.

Table 3-30 DPTX signal descriptions

Signal name	Type	Description	Ball location
DP_LN0_TXN	AIO	DPTX lane 0 (negative)	AH35
DP_LN0_TXP	AIO	DPTX lane 0 (positive)	AG35
DP_LN1_TXN	AIO	DPTX lane 1 (negative)	AH31
DP_LN1_TXP	AIO	DPTX lane 1 (positive)	AH32
DP_LN2_TXN	AIO	DPTX lane 2 (negative)	AJ33
DP_LN2_TXP	AIO	DPTX lane 2 (positive)	AJ34
DP_LN3_TXN	AIO	DPTX lane 3 (negative)	AK31
DP_LN3_TXP	AIO	DPTX lane 3 (positive)	AK32
DP_TX_HPD	DI	DPTX hot plug detect	AB33, J31, Y9, AA11, E5

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Signal name	Type	Description	Ball location
DPAUXN	AIO	DPTX auxiliary channel (negative)	AJ37
DPAUXP	AIO	DPTX auxiliary channel (positive)	AJ36

3.8.4 Embedded DisplayPort Interface (EDPTX)

The EDPTX provides the electrical transport for video and auxiliary data between the device and an external display module. The communication link is handled through the eDP Auxiliary Channel (EDPAUX).

The EDPTX supports the following key features:

- Compliance with eDP v1.2 standard
- Single link output port with 2× main lanes
- Up to 5.4 Gbps per lane (HBR3)
- Hot Plug Detect (HPD)
- Auxiliary channel lane:
  - Manchester-II coding
  - clock extracted from the data stream
  - 1 Mbps bit rate
- Input data formats: RGB 8-bit/10-bit, YUV422 8-bit/10-bit
- Output data format: RGB444 8-bit/10-bit, YCbCr422 8-bit/10-bit
- 8-bit to 10-bit encoder
- Interlane skew function
- Up to 1920 × 1440 @ 60 Hz resolution (10-bit)

3.8.4.1 EDPTX Signal Descriptions

Table 3-31 presents EDPTX signal descriptions.

Table 3-31 EDPTX signal descriptions

Signal name	Type	Description	Ball location
EDP_TX_HPD	DI	EDPTX hot plug detect	AC32, AA35, F4, AA7, Y5, K30
EDP_LN0_TXN	AIO	EDPTX lane 0 (negative)	AG29
EDP_LN0_TXP	AIO	EDPTX lane 0 (positive)	AG30
EDP_LN1_TXN	AIO	EDPTX lane 1 (negative)	AF31
EDP_LN1_TXP	AIO	EDPTX lane 1 (positive)	AF32
EDPAUXN	AIO	EDPTX auxiliary channel (negative)	AF37
EDPAUXP	AIO	EDPTX auxiliary channel (positive)	AF36

3.8.5 High-Definition Multimedia Interface Transmitter (HDMITX)

The HDMITX module encodes video, audio and control data into Transition-Minimized Differential Signaling (TMDS) format for digital transmission based on HDMI Specification 2.0b, and transfers the uncompressed digital data streams to an HDMI compatible sink device.

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The HDMITX supports the following video features:

- Deep Color mode: up to 16 bits
- Maximum operating frequency: 594 MHz (4096 × 2160p @ 60 Hz, 8-bit mode)
- Video color space options: RGB 444, YCbCr 4:2:2 (ITU 601 and 709), YCbCr 4:4:4 (ITU 601 and 709), YCbCr 4:2:0, and xvYCC
- 3D HDMI function
- SD mode resolutions:
  - 1440 × 480i (pixel repeat 2) @ 59.94/60 Hz
  - 720 × 480p @ 59.94/60 Hz
  - 1440 × 576i (pixel repeat 2) @ 50 Hz
  - 720 × 576p @ 50 Hz
- HD/FHD/UFHD mode resolutions:
  - 1280 × 720p @ 59.94/60/50 Hz
  - 1920 × 1080i @ 59.94/60/50 Hz
  - 1920 × 1080p @ 59.94/60/50 Hz
  - 1920 × 1080p @ 23.97/24 Hz
  - 1920 × 1080p @ 25 Hz
  - 1920 × 1080p @ 29.97/30 Hz
  - 3840 × 2160p @ 29.97/30 Hz
  - 3840 × 2160p @ 59.94/60/50 Hz

The HDMITX supports the following audio features:

- Single compressed S/PDIF IEC61937 (up to 192 kHz)
- Single LPC SPDIF IEC60958 (up to 192 kHz and up to 24 bits), 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, 192 kHz
- Multi-channel PCM input (maximum 8 channels)
- Direct Stream Digital (DSD) audio
- Compressed lossless audio according to HDMI 2.0

Additionally, the HDMITX supports the following general features:

- Hot Plug Detect (HPD) line
- Discovery by Extended Display Identification Data (EDID)
- Compatible with Digital Visual Interface (DVI) 1.0
- High-bandwidth Digital Content Protection (HDCP) 1.4/HDCP 2.3 function
- Support of dynamic metadata maximum to 2 KB
- I²C-based Display Data Channel (DDC) with clock stretching
- Variable Refresh Rate (VRR)/Auto Low Latency Mode (ALLM)
- Support Consumer Electronics Control (CEC) function

3.8.5.1.1 HDMITX Signal Descriptions

Table 3-32 presents HDMITX signal descriptions.

Table 3-32 HDMITX signal descriptions

Signal name	Type	Description	Ball location
HDMITX20_CEC	DIO	HDMITX CEC channel	AC33, T30

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Signal name	Type	Description	Ball location
HDMITX20_HTPLG	DI	HDMITX HPD line	R31, AC32
HDMITX20_PWR5V	DO	HDMITX power supply (+5 V)	AB32, AB34
HDMITX20_SCL	DIO	HDMITX DDC/I2C clock	T31, AD32
HDMITX20_SDA	DIO	HDMITX DDC/I2C data	AD33, U32
HDMITX21_CH0_M	AO	HDMITX TMDS data lane 0 (negative)	AN34
HDMITX21_CH0_P	AO	HDMITX TMDS data lane 0 (positive)	AN35
HDMITX21_CH1_M	AO	HDMITX TMDS data lane 1 (negative)	AM37
HDMITX21_CH1_P	AO	HDMITX TMDS data lane 1 (positive)	AM36
HDMITX21_CH2_M	AO	HDMITX TMDS data lane 2 (negative)	AL35
HDMITX21_CH2_P	AO	HDMITX TMDS data lane 2 (positive)	AK35
HDMITX21_CLK_M	AO	HDMITX TMDS clock lane (negative)	AR35
HDMITX21_CLK_P	AO	HDMITX TMDS clock lane (positive)	AR34

3.8.6 Warp Engine (WPE)

The WPE provides image geometry warping function which can be standalone or in-line linked with SVPP-0. The WPE uses backward mapping method to process lens distortion. WPE reads image data from DRAM and outputs image data to DRAM.

The WPE supports the following key features:

- Input/output color formats:
  - Y/U/V only 8-/10-bit
  - UV420 8-/10-bit
  - UV422 8-/10-bit
  - YUV420 8-/10-bit (including of Arm Frame Buffer Compression (AFBC) format)
  - YUV422 8-/10-bit
  - YUV444 8-/10-bit (Output only)
  - AYUV444 8bit (Output only)
  - RGB888 (Output only)
  - ARGB8888 (Output only)
- Input/output color range: Full 8-bit (0-255), or 10-bit (0-1023)
- Input/output maximum image size: 8000 × 6000
- Output color space convertor
- Frame rate: 30fps
- WarpMap size: From 2×2 up to 640 × 480
- Latency (one frame delay): 33 ms
- Interpolation methods:
  - Bi-linear interpolation for WarpMap processing
  - Bi-cubic filtering for output image processing
- WPE cache size: 32KB

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3.8.7 Multimedia SRAM (MMSYSRAM)

The MMSYSRAM is a shared SRAM used by some modules in the video and display data paths, such as VENC，CAMSYS and MCUSYS/APUSYS.

The MMSYSRAM supports the following main features:

- Size: 768 KB
- Address Protection Controller (APC)
- Memory Protection Unit (MPU)
- Up to 8 masters at the same time
- Up to 8 regions split

3.8.8 In-Line Rotation Controller (INLINEROT)

The INLINEROT module is used by MDP_WROT and DISP_RDMA to exchange data through MMSYSRAM in order to decrease DRAM transactions bandwidth.

3.9 Imaging

The Camera Imaging Subsystem (CAMSYS) is built around a feature-rich Image Signal Processor (ISP) and a deep learning Face Detection (FD) engine. The ISP processes data received either from camera sensors through MIPI CSI-2 interface or system DRAM.

3.9.1 Camera Image Signal Processing (ISP)

The ISP consists of two engines—a real-time engine (pass 1) and an offline engine (pass 2). The processed data is stored into system DRAM.

The ISP supports the following key features:

- Single camera capture: up to 32 MP at 30 fps
- Dual camera capture: up to 16 MP + 16 MP at 30 fps
- Video High Dynamic Range (HDR) with stagger HDR sensor: up to 16 MP at 30 fps
- Full size image capture for preview
- Image processing functions:
  - Auto sensor defect pixel correction
  - Lens shading correction
  - Edge enhancement
  - Video stabilization
  - Motion compensated temporal noise reduction for video recording
  - Electronic image stabilization
  - Multiple-frame noise reduction for image capture
  - Zero shutter delay image capture
  - Preference color adjustment
  - AE/AWB/AF statistics collection
  - Two-frame stagger HDR fusion
  - Anti-blooming correction
  - YUV frame buffer compression

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3.9.1.1 Camera Signal Descriptions

Table 3-33 presents camera signal descriptions.

Table 3-33 Camera signal descriptions

Signal name	Type	Description	Ball location
CMFLASH0	DO	Camera flash strobe 0	AC7, V4, G4
CMFLASH1	DO	Camera flash strobe 1	V5, G3, AB4
CMFLASH2	DO	Camera flash strobe 2	AA35, J31, E3
CMFLASH3	DO	Camera flash strobe 3	G5, Y11, K30,
CMMCLK0	DO	Sensor reference clock 0	E4
CMMCLK1	DO	Sensor reference clock 1	E5
CMMCLK2	DO	Sensor reference clock 2	F4
CMVREF0	DO	Camera frame sync 0	V6, AD11, W4
CMVREF1	DO	Camera frame sync 1	AD10, W5, T11
CMVREF2	DO	Camera frame sync 2	AB2, V7, AA11
CMVREF3	DO	Camera frame sync 3	AB1, V8, Y5
CMVREF4	DO	Camera frame sync 4	G36, U7, G4
CMVREF5	DO	Camera frame sync 5	U8, H36, G3
CMVREF6	DO	Camera frame sync 6	T9, J36, W8
CMVREF7	DO	Camera frame sync 7	T10, J37, AA35

3.9.2 Face Detection (FD)

The Face Detection (FD) engine uses a convolutional neural network algorithm to detect faces on a source image and output the detected coordinates of the face windows and their confidence values.

The FD engine supports the following key features:

- Input image formats:
  - YUV420: 2 plane
  - YUV422: 2 plane (Y/UV, Y/VU)
  - YUV422: 1 plane (YUYV, YVYU, UYVY, VYUY)
- YUV to RGB888 format conversion
- Image up/down-scaling
  - Maximum resize width: 640 pixels

3.9.3 Camera Serial Interface

The CSI is based on MIPI Alliance Specification for Camera Serial Interface 2 (MIPI CSI-2) Version 2.1. The CSI provides high-speed serial data transfer between the ISP and external camera image sensors.
The device features two MIPI CSI-2 controllers (CSI0 and CSI1), which are fully compliant with the MIPI CSI-2 specification.

The CSI0 controller and the CSI1 controller utilize a combined MIPI D-PHY/C-PHY physical layer. The PHY layer is based on MIPI D-PHY Specification Revision 2.1, MIPI C-PHY Specification Revision 1.2 and acts as a physical link between the CSI controllers and image sensors.

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The MIPI CSI-2 implementation in the device provides the following key features:

- Primary CSI-2 interface (CSI0), which can be used in the following configuration:
  - One 4-data lane interface in D-PHY mode, or
  - Two 2-data lane interfaces in D-PHY mode, or
  - One 3-trio interface in C-PHY mode, or
  - Two 2-trio interfaces in C-PHY mode
- Secondary CSI-2 interface (CSI1), which can be used in one of the following configurations:
  - One 4-data lane interface in D-PHY mode, or
  - One 3-trio interface in C-PHY mode
- Pixel formats: RAW8/RAW10/RAW12/RAW14/YUV422 8-bit
- No support for D-PHY escape mode and bus turnaround

3.9.3.1 CSI Signal Descriptions

Table 3-34 presents CSI0 signal descriptions.

Table 3-34 CSI0 signal descriptions

Signal name	Type	Description				Ball location
		1× D-PHY 4-lane Mode	2 × D-PHY 2-lane Mode	1 × C-PHY 3-trio Mode	2 × C-PHY 2-trio Mode	
CSI0A_L0N_T0B	AIO	CSI0 data lane 2 (negative)	CSI0 port 0 data lane 0 (negative)	CSI0 Trio0 B	CSI0 Trio0 B	N3
CSI0A_L0P_T0A	AIO	CSI0 data lane 2 (positive)	CSI0 port 0 data lane 0 (positive)	CSI0 Trio0 A	CSI0 Trio0 A	N2
CSI0A_L1N_T1A	AIO	CSI0 data lane 0 (negative)	CSI0 clock lane (negative)	CSI0 Trio1 A	CSI0 Trio1 A	N5
CSI0A_L1P_T0C	AIO	CSI0 data lane 0 (positive)	CSI0 clock lane (positive)	CSI0 Trio0 C	CSI0 Trio0 C	N4
CSI0A_L2N_T1C	AIO	CSI0 clock lane (negative)	CSI0 port 0 data lane 1 (negative)	CSI0 Trio1 C	CSI0 Trio1 C	N6
CSI0A_L2P_T1B	AIO	CSI0 clock lane (positive)	CSI0 port 0 data lane 1 (positive)	CSI0 Trio1 B	CSI0 Trio1 B	M6
CSI0B_L0N_T0B	AIO	CSI0 data lane 1 (negative)	CSI0 port 0 data lane 0 (negative)	CSI0 Trio2 B	CSI0 Trio2 B	P1
CSI0B_L0P_T0A	AIO	CSI0 data lane 1 (positive)	CSI0 port 0 data lane 0 (positive)	CSI0 Trio2 A	CSI0 Trio2 A	P2
CSI0B_L1N_T1A	AIO	CSI0 data lane 3 (negative)	CSI0 clock lane (negative)	-	CSI0 Trio1 A	P4
CSI0B_L1P_T0C	AIO	CSI0 data lane 3 (positive)	CSI0 clock lane (positive)	CSI0 Trio2 C	CSI0 Trio0 C	P3
CSI0B_L2N_T1C	AIO	-	CSI0 port 0 data lane 1 (negative)	-	CSI0 Trio1 C	P6
CSI0B_L2P_T1B	AIO	-	CSI0 port 0 data lane 1 (positive)	-	CSI0 Trio1 B	P5

1. Unused CSI ports could be connected to GND or set in not connected.

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Table 3-35 presents CSI1 signal descriptions.

Table 3-35 CSI1 signal descriptions

Signal name	Type	Description		Ball location
		1 × D-PHY 4-lane Mode	1 × C-PHY 3-trio Mode	
CSI1A_L0N_T0B	AIO	CSI1 data lane 2 (negative)	CSI1 Trio0 B	J4
CSI1A_L0P_T0A	AIO	CSI1 data lane 2 (positive)	CSI1 Trio0 A	J5
CSI1A_L1N_T1A	AIO	CSI1 data lane 0 (negative)	CSI1 Trio1 A	J3
CSI1A_L1P_T0C	AIO	CSI1 data lane 0 (positive)	CSI1 Trio0 C	J2
CSI1A_L2N_T1C	AIO	CSI1 clock lane (negative)	CSI1 Trio1 C	K6
CSI1A_L2P_T1B	AIO	CSI1 clock lane (positive)	CSI1 Trio1 B	K7
CSI1B_L0N_T0B	AIO	CSI1 data lane 1 (negative)	CSI1 Trio2 B	K3
CSI1B_L0P_T0A	AIO	CSI1 data lane 1 (positive)	CSI1 Trio2 A	K5
CSI1B_L1N_T1A	AIO	CSI1 data lane 3 (negative)	-	L4
CSI1B_L1P_T0C	AIO	CSI1 data lane 3 (positive)	CSI1 Trio2 C	L3

1. Unused CSI ports could be connected to GND or set in not connected.

3.9.3.2 CSI Timing Characteristics

The CSI interface timing characteristics are compliant with MIPI CSI-2 Specification v2.1, MIPI D-PHY Specification v2.1, and MIPI C-PHY Specification v1.2.

3.10 Video

3.10.1 Video Encoder (VENC)

The VENC accelerator supports main stream H.264 and HEVC video encoding. It is capable of encoding 4K video at 30 fps superior video quality. The VENC supports various encoding methods that satisfy basic requirements of easy control by software. The VENC brings astonishing high quality and low memory bandwidth requirements, with advanced encoding technology. The accelerator also considers the usage of portable devices and provides several power saving capabilities.

The VENC has the following main features:

- Uses DRAM as an input, output, and working buffer
- Reads input frame buffers, executes video encoding and writes encoded bit stream to the output buffer
- Support of YUV420 two-plane scan line (NV12/NV21) and YUV420 three-plane scan line (YV12/I420) color spaces

Table 3-36 presents the supported video formats and their capabilities.

Table 3-36 VENC supported formats

Format	Feature	Details
H. 264 Encoding	Profile	Main (8-bit)
	Level	L4.1
	Speed	4K@30fps
HEVC Encoding	Profile	Main (8-bit)
	Level	L4.1
	Speed	4K@30fps

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3.10.2 Video Decoder (VDEC)

The VDEC accelerator provides multi-standard video decoding feature. The main purpose of the accelerator is to relieve CPU usage while providing high performance video decompression. The input to VDEC is a compressed video bitstream. After decoding process, the reconstructed video is written into DRAM and then sent to the display subsystem.

The VDEC supports various multimedia video formats, including:

- HEVC decoder:
  - Main profile / Main 10 profile
  - Maximum level: L5.1
  - 4K2K @ 75fps (160 Mbps)
- H.264 decoder:
  - Baseline Profile (BP) / Main profile / High profile / High 10 profile
  - Maximum level: L5.2
  - 4K2K @ 75fps (160 Mbps)
- MPEG-4 decoder:
  - Simple Profile (SP)
    - Maximum level: L6
    - 1080p @ 60 fps (60 Mbps)
  - Advanced Simple Profile (ASP)
    - Maximum level: L5
    - 1080p @ 60 fps (60 Mbps)
- MPEG-2 decoder:
  - Main profile
  - Maximum level: High
  - 1080p @ 60 fps (60 Mbps)
- VP8 decoder:
  - 1080p @ 60 fps (40 Mbps)
- VP9 decoder:
  - Profile 0 / profile 2
  - 4K2K @ 75 fps (120 Mbps)
- AV1 decoder:
  - Main profile
  - Maximum level: L5.1
  - 4K2K @ 75 fps (120 Mbps)
- H.263 decoder:
  - Baseline profile
  - 1080p @ 60 fps (60 Mbps)
- High Efficiency Image File (HEIF) format decoder:
  - Main profile / Main10 profile
  - Maximum resolution 16383 × 16383
- Error handling

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3.10.2.1 Interface

The output format supported by VDEC is:

- NV12_BLK (Video block mode), 420 format block mode, 2 plane (UV)
- NV12_BLK_FCM (video field compact mode), 420 format block mode, 2 plane (UV)

VDEC uses DRAM as bitstream input, working buffer, reference buffer and output, and DRAM access process is achieved by using SMI interface. Seven sets of SMI interfaces with 128 bits of read/write are used, including MC/PP/PP_WRAP/AVC_MV/PRED_RD/PRED_WR/VLD. In addition, all ports are EMI ports, i.e. no SYSRAM is required.

Register settings are passed to VDEC by APB interface. There is one set of APB interfaces.

3.11 Audio

The audio subsystem provides audio data exchange between the device and external audio components. The device has the following audio interfaces:

- One master I^2S output:
  - 2-channel I^2S output. Sampling rates from 8 kHz to 192 kHz, up to 32 bits
  - 16-channel Time Division Multiplexing (TDM) output. Sampling rates from 8 kHz to 48 kHz, up to 32 bits
- One master or slave I^2S output:
  - 8-channel I^2S output. Sampling rates from 8 kHz to 192 kHz, up to 32 bits
  - 16-channel TDM output with 48 kHz sampling rate
- One master or slave I^2S input:
  - 8-channel I^2S input. Sampling rates from 8 kHz to 192 kHz and resolution up to 32 bits
  - 16-channel TDM input. Sampling rates from 8 kHz to 48 kHz, up to 32 bits, or 16-channel direct path to memory
- One master or slave TDM input:
  - 16-channel TDM output with 48 kHz sampling rate and bit resolution up to 32 bits
  - 2-channel I^2S input. Sampling rates from 8 kHz to 192 kHz and resolution up to 32 bits
- One master 8-channel High-Definition Multimedia Interface (HDMI™) audio output (HDMITX):
  - Sampling rates from 8 kHz to 192 kHz with resolution of up to 32 bits
  - 8-channel DisplayPort™ audio output with sampling rates from 8 kHz to 192 kHz, up to 24 bits
- One S/PDIF input. Sampling rates include 32, 44.1, 48, 88.2, 96, 176.4, and 192 kHz
- One S/PDIF output with 32, 44.1, 48, 88.2, 96, 176.4, and 192 kHz sampling rates
- One master or slave PCM interface with Sampling Rate Converter (SRC). Supported sampling rates: 8, 16, 32, 44.1, and 48 kHz
- One slave 8-channel I^2S input (AUDIO IN)
- 4 × Pulse Density Modulation (PDM) interfaces for up to 4 stereo Digital Microphones (DMICs). Support of one-wire and two-wire modes with 8, 16, 32, and 48 kHz PCM sampling rates and 24 bits
- A proprietary audio interface for PMIC CODEC
  - 2-channel DAC. Supports up to 192 kHz sampling rate
  - 2-channel ADC. Supports up to 192 kHz sampling rate

Audio subsystem features:

- Audio playing
  - Support of 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48, 88.2, 96, 176.4, 192 kHz sampling rates

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- Audio recording
  - Support of 8, 16, 32, 48, 96, and 192 kHz sampling rates
  - Support of recording of up to 8-channel audio data
- 12 × stereo general-purpose Asynchronous Sample Rate Converters (ASRC) for sampling rate conversion and slave mode clock tracking
- 4 × stereo memory-based ASRC
- 2 × stereo hardware gain
- 32-channel channel merge
- 5 × APLL can support up to 5 clock rates at the same time
- 64KB internal audio SRAM
- Voice wakeup

Figure 3-22 shows the Audio interfaces block diagram.

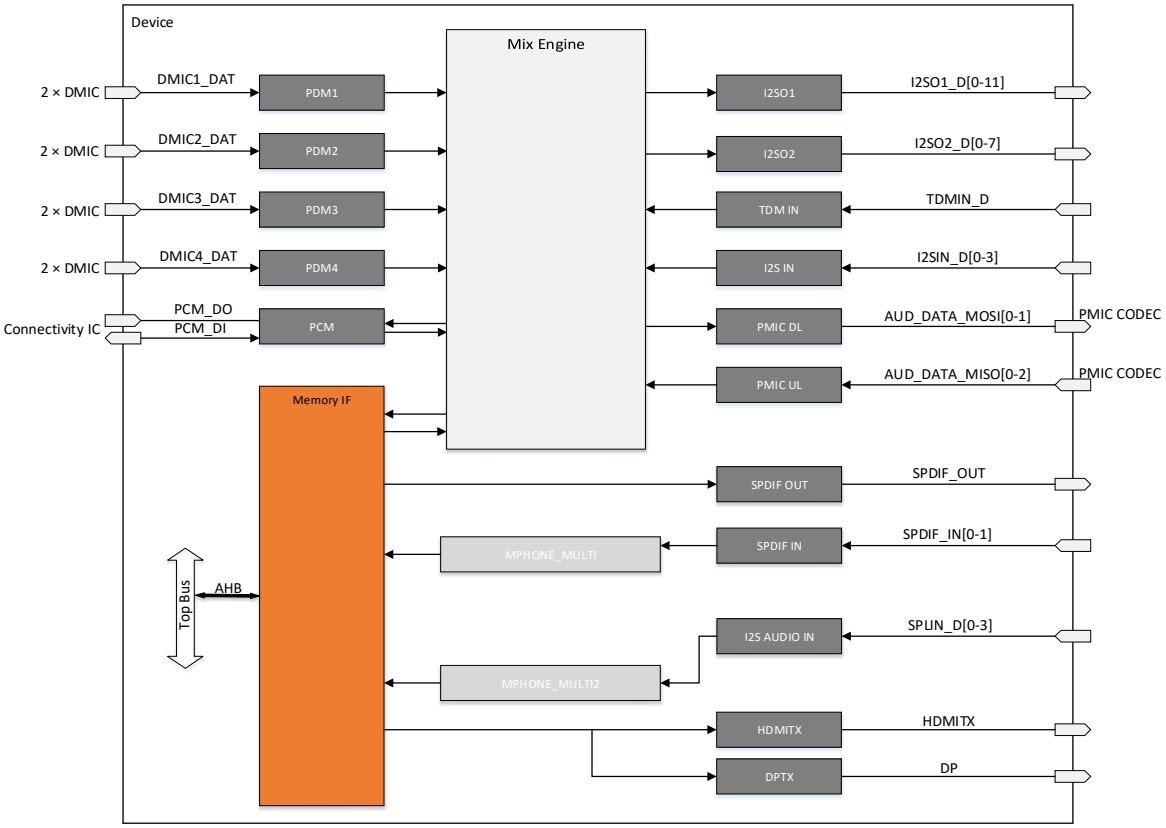

Figure 3-22 Audio interfaces block diagram

3.11.1 Inter-IC Sound (I2S)

3.11.1.1 I2S Signal Descriptions

Table 3-37 presents I2S signal descriptions.

Table 3-37 I2S signal descriptions

Signal name	Type	Description	Ball location
I2SIN			
I2SIN_BCK	DIO	I2SIN serial bit clock	M33, H36, H33, U10
I2SIN_D0	DI	I2SIN serial data input 0	J37, J33, M34, Y7

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Signal name	Type	Description	Ball location
I2SIN_D1	DI	I2SIN serial data input 1	G33, G31, N33, Y8
I2SIN_D2	DI	I2SIN serial data input 2	G32, G30, M30, W7
I2SIN_D3	DI	I2SIN serial data input 3	H35, H32, M32, W3
I2SIN_MCK	DIO	I2SIN master clock	H34, K30, Y10, G36
I2SIN_WS	DIO	I2SIN word select (left/right audio channel)	J34, M35, Y6, J36
I2SO1			
I2SO1_BCK	DO	I2SO1 serial bit clock	W7, G1, AD10, H32, M35
I2SO1_D0	DO	I2SO1 serial data output 0	N33, W8, E2, AB1, H35
I2SO1_MCK	DO	I2SO1 master clock	Y8, G2, M33, G30, AD11
I2SO1_WS	DO	I2SO1 word select (left/right audio channel)	F2, AB2, G32, M34, W3
I2SO2			
I2SO2_BCK	DIO	I2SO2 serial bit clock	AC9, U10, H33
I2SO2_D0	DO	I2SO2 serial data output 0	AC4, Y7, J33
I2SO2_D1	DO	I2SO2 serial data output 1	AB3, Y8, G31
I2SO2_D2	DO	I2SO2 serial data output 2	AA8, W7, G30
I2SO2_D3	DO	I2SO2 serial data output 3	AC8, W3, H32
I2SO2_MCK	DO	I2SO2 master clock	Y10, H34, AB9
I2SO2_WS	DIO	I2SO2 word select (left/right audio channel)	Y6, J34, AB8
SPLIN			
SPLIN_BCK	DI	SPLIN serial bit clock	J36
SPLIN_D0	DI	SPLIN data 0	J37
SPLIN_D1	DI	SPLIN data 1	G33
SPLIN_D2	DI	SPLIN data 2	G32
SPLIN_D3	DI	SPLIN data 3	H35
SPLIN_LRCK	DI	SPLIN word select	H36
SPLIN_MCK	DI	SPLIN master clock	G36

3.11.1.2 I2S Timing Characteristics

Table 3-38 and Figure 3-23 present timing characteristics for the I2S modules in the device.

Table 3-38 I2S timing characteristics

No.	Parameter	Description	Min.	Typ.	Max.	Unit
-	f_S	Sampling frequency	8		192	kHz
IIS01	f_{c_MCK}	Cycle time, MCK (master clock)	-	-	24.576	MHz
-	f_{OP_BCK}	Operation frequency, BCK	32 × f_S	-	64 × f_S	MHz
IIS03	t_{c_BCK}	Cycle time, BCK	81.38		3906.25	ns
IIS04	$t_{w\_BCK\_H}$	Pulse duration, BCK high	-	0.5	-	1 / t_{c_BCK}
IIS05	$t_{w\_BCK\_L}$	Pulse duration, BCK low	-	0.5	-	1 / t_{c_BCK}
-	t_{LRCK}	LRCK period	32	-	64	1 / t_{c_BCK}
IIS06	t_{v_LRCK}	BCK negative edge to LRCK valid	-	-	19	ns
IIS07	t_{v_DO}	BCK negative edge to DO valid	-	-	19	ns
IIS08	t_{su}	Setup time, DI	19	-	-	ns
IIS10	t_h	Hold time, DI	19	-	-	ns

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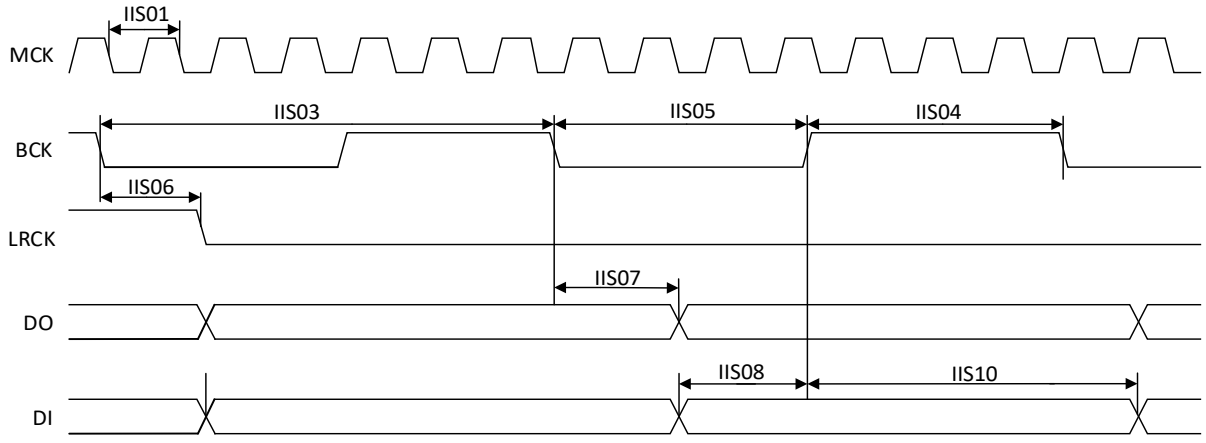

Figure 3-23 I2S master mode timing diagram

3.11.2 Pulse-Code Modulation (PCM)

3.11.2.1 PCM Signal Descriptions

Table 3-39 presents PCM signal descriptions.

Table 3-39 PCM signal descriptions

Signal name	Type	Description	Ball location
PCM_CLK	DIO	PCM clock	G1, AD30
PCM_DI	DI	PCM data input	E2, AB31
PCM_DO	DO	PCM data output	AC30, F2
PCM_SYNC	DIO	PCM synchronization	AC31, G2

3.11.2.2 PCM Timing Characteristics

Table 3-40, Figure 3-24 and Figure 3-25 present timing characteristics for the PCM interfaces in the device.

Table 3-40 PCM timing characteristics

No.	Parameter	Description	Min.	Typ.	Max.	Unit
	f_S	Sampling frequency	8	-	48	kHz
PCM1	f_{CLK}	Serial clock frequency	0.256	-	3.072	MHz
	t_{SYNC}	Sync period	32	-	64	$1 / f_{CLK}$
PCM2	$t_{w\_CLK\_H}$	Pulse duration, CLK high	-	0.5	-	$1 / f_{CLK}$
PCM3	$t_{w\_CLK\_L}$	Pulse duration, CLK low	-	0.5	-	$1 / f_{CLK}$
PCM4	$t_{d\_CLK\_SYNC}$	Delay time, output CLK low to SYNC valid	-	-	78	ns
PCM5	$t_{d\_CLK\_TX}$	Delay time, output CLK low to TX valid	-	-	78	ns
PCM6	t_{su}	Setup time, RX master mode	78	-	-	ns
PCM7	t_h	Hold time, RX master mode	78	-	-	ns
PCM8	t_{su}	Setup time, RX slave mode	78	-	-	ns
PCM9	t_h	Hold time, RX slave mode	78	-	-	ns

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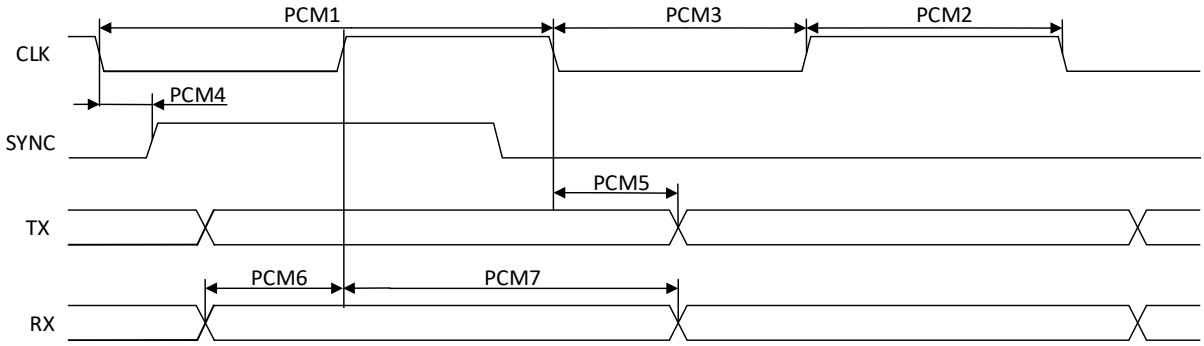

Figure 3-24 PCM master mode timing diagram

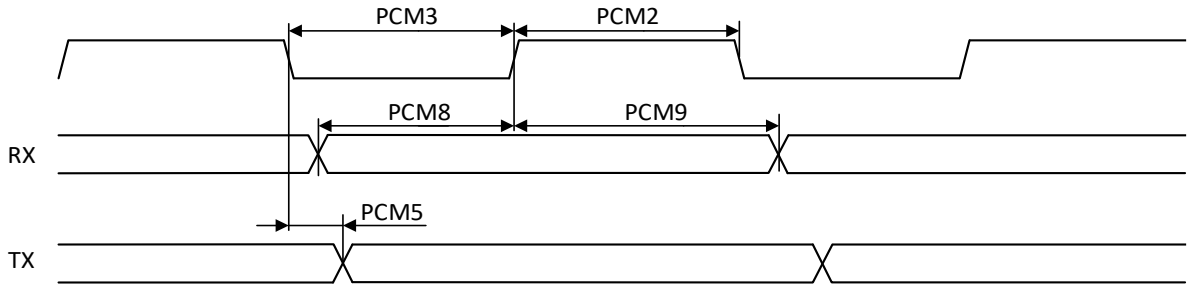

Figure 3-25 PCM slave mode timing diagram

3.11.3 Time Division Multiplexed (TDM) Interface

3.11.3.1 TDM Signal Descriptions

Table 3-41 presents TDM signal descriptions.

Table 3-41 TDM signal descriptions

Signal name	Type	Description	Ball location
TDMIN_BCK	DIO	TDM clock	AD35, W5, T10, N31, G3, H35
TDMIN_DI	DI	TDM receive data input	AD36, V5, T7, N34, G5, H32
TDMIN_LRCK	DIO	TDM word select (left/right audio channel)	V4, T8, P30, E3, G30, AD37
TDMIN_MCK	DIO	TDM receive master clock	T9, N30, G4, G32, AC35, W4

3.11.3.2 TDM Timing Characteristics

Table 3-42 and Figure 3-26 present timing characteristics for the TDM interfaces in the device.

Table 3-42 TDM timing characteristics

No.	Parameter	Description	Min.	Typ.	Max.	Unit
	f_S	Sampling frequency	8	-	192	kHz
TDM1	f_{MCK}	Master clock frequency	-	-	24.576	MHz
TDM2	f_{BCK}	Serial clock frequency	0.256	-	24.576	MHz
TDM3	$t_{w\_BCK\_H}$	Pulse duration, BCK high	-	0.5	-	1 / f_{BCK}
TDM4	$t_{w\_BCK\_L}$	Pulse duration, BCK low	-	0.5	-	1 / f_{BCK}
TDM5	$t_{d\_BCLK\_WS}$	Delay time, output BCLK low to WS valid	-	-	10	ns
TDM6	$t_{d\_BCLK\_DO}$	Delay time, output BCLK low to SDOUT valid	-	-	10	ns

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No.	Parameter	Description	Min.	Typ.	Max.	Unit
TDM7	t_{su_DI}	Setup time, SDIN	10	-	-	ns
TDM8	t_{h_DI}	Hold time, SDIN	10	-	-	ns

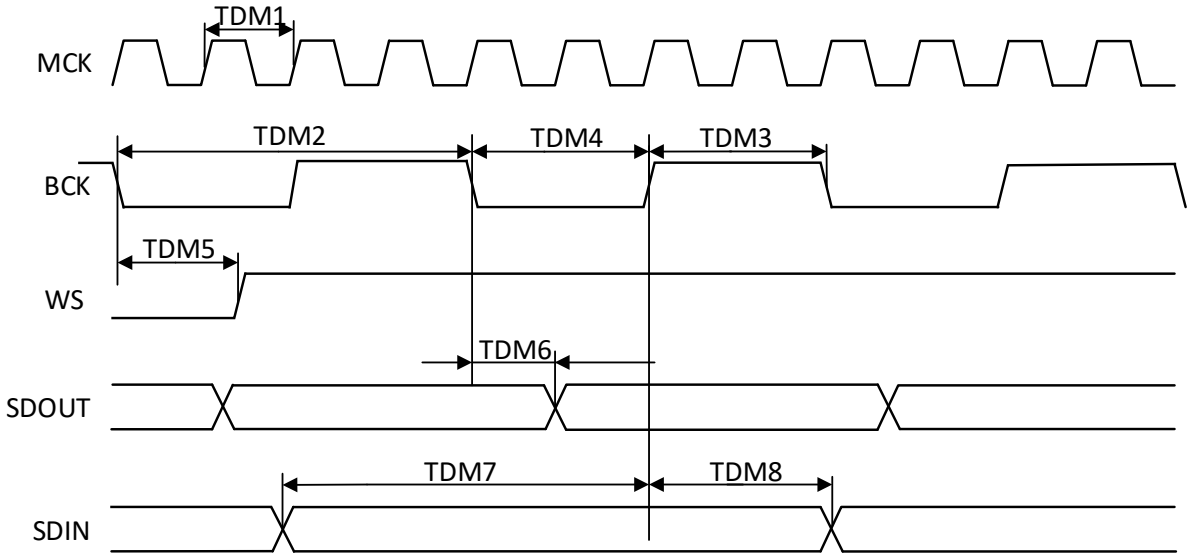

Figure 3-26 TDM master mode timing diagram

3.11.4 Pulse Density Modulation (PDM)

3.11.4.1 PDM Timing Characteristics

Table 3-43 and Figure 3-27 present timing characteristics for the PDM interface in the device.

Table 3-43 PDM timing characteristics

No.	Parameter	Description	Min.	Typ.	Max	Unit
	f_{CLK}	Operating frequency, PDM CLK	0.40625	-	3.25	MHz
PDM2	$t_{W\_CLK\_H}$	Pulse duration, CLK high	-	0.5	-	1 / f_{CLK}
PDM3	$t_{W\_CLK\_L}$	Pulse duration, CLK low	-	0.5	-	1 / f_{CLK}
PDM4	t_{SU_DAT}	Setup time, DAT	0.2	-	-	1 / f_{CLK}
PDM5	t_{H_DAT}	Hold time, DAT	0.2	-	-	1 / f_{CLK}

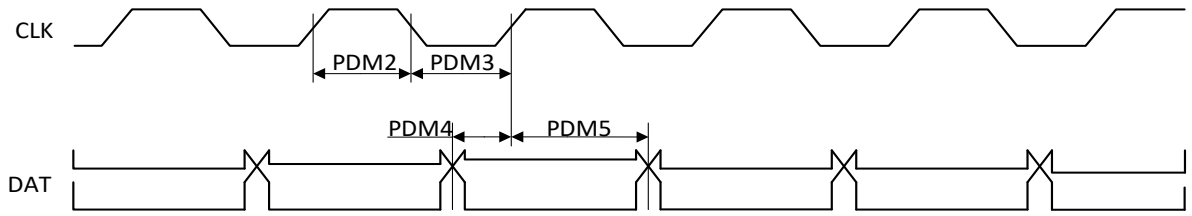

Figure 3-27 PDM timing diagram

3.11.5 Digital Microphone (DMIC)

3.11.5.1 DMIC Signal Descriptions

Table 3-44 presents DMIC signal descriptions.

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Table 3-44 DMIC signal descriptions

Signal name	Type	Description	Ball location
DMIC1_CLK	DO	DMIC1 clock	AB9, W3, N30
DMIC1_DAT	DI	DMIC1 data in one-wire mode or data left	AC9, W4, N31
DMIC1_DAT_R	DI	DMIC1 data right	AB8, W5, P30
DMIC2_CLK	DO	DMIC2 clock	V4, N34, AC4
DMIC2_DAT	DI	DMIC2 data in one-wire mode or data left	P33, AB3, V5
DMIC2_DAT_R	DI	DMIC2 data right	P35, AA8, W8
DMIC3_CLK	DO	DMIC3 clock	V6, G33, AC8, Y10
DMIC3_DAT	DI	DMIC3 data in one-wire mode or data left	U10, T11, G32, AB7
DMIC3_DAT_R	DI	DMIC3 data right	Y6, V7, H35, AB6
DMIC4_CLK	DO	DMIC4 clock	Y7, V8, H36, AB5
DMIC4_DAT	DI	DMIC4 data in one-wire mode or data left	Y8, U7, J36, AC5
DMIC4_DAT_R	DI	DMIC4 data right	AA5, W7, U8, J37

3.11.6 Digital Interface (SPDIF)

3.11.6.1 SPDIF Signal Descriptions

Table 3-45 presents SPDIF signal descriptions.

Table 3-45 SPDIF signal descriptions

Signal name	Type	Description	Ball location
SPDIF_IN0	DI	SPDIF input 0	AD10, W3, D4, G36
SPDIF_IN1	DI	SPDIF input 1	AB2, W7, D2, P33
SPDIF_IN2	DI	SPDIF input 2	D1, P35, AB1, Y8
SPDIF_OUT	DO	SPDIF output	W8, D3, G33, AD11

3.11.7 Power Management Integrated Circuit (PMIC)

3.11.7.1 PMIC Audio Interface Signal Descriptions

Table 3-46 presents PMIC audio interface signal descriptions.

Table 3-46 PMIC audio interface signal descriptions

Signal name	Type	Description	Ball location
AUD_CLK_MOSI(1)	DO	PMIC CODEC clock master output	M33
AUD_DAT_MISO0	DI	PMIC CODEC data master input 0	M30
AUD_DAT_MISO1	DI	PMIC CODEC data master input 1	M32
AUD_DAT_MOSI0	DO	PMIC CODEC data master output 0	M34
AUD_DAT_MOSI1	DO	PMIC CODEC data master output 1	N33
AUD_SYNC_MOSI	DO	PMIC CODEC sync master output	M35

1. These pins should be left unconnected when unused.

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3.12 Connectivity

3.12.1 Inter-Integrated Circuit (I2C) and Improved I2C (I3C)

The device contains five I2C and two I3C controllers providing an interface between the internal hosts and any I2C™ or MIPI I3C® bus compatible devices.

Each I2C module supports the following key features:

- Compliant with Philips I²C-bus Specification version 2.1
- Standard-Speed (SS) communication mode (up to 100 Kbps)
- Fast-Speed (FS) communication mode (up to 400 Kbps)
- Fast-Speed Plus (FS+) communication mode (up to 1 Mbps)
- High-Speed (HS) communication mode (up to 3.4 Mbps)
- Adjustable clock speed for LS and FS modes
- Support slave clock extension
- Master mode of operation
- Support of manual transfer mode
- Multi-byte writes and reads per transfer
- Multi-byte write and read messages per transfer
- Active drive/wired-and I/O configuration
- Combined format transfer with length change capability
- Multi-transfer per transaction
- Repeated START condition in multiple transfer

Each I3C module supports the following additional features:

- Single Data Rate (SDR) transfer
- Dynamic Address Assignment (DAA)
- Common Command Code (CCC)

The I2C/I3C controller is designed to monitor when the SCL and SDA signals are low to turn off the internal pull-up resistance, thus saving power.

I2C/I3C PAD control supports:

- Eight settings of internal pull-up resistance: 1 kΩ, 1.5 kΩ, 2 kΩ, 3 kΩ, 4 kΩ, 5 kΩ, 10 kΩ (POR default), and 75 kΩ
- Four open-drain drive strengths: 0.31 mA, 0.63 mA, 1.12 mA, and 1.43 mA
- The IO_CONFIG register must be configured to 0x33 for open-drain

3.12.1.1 I2C/I3C Signal Descriptions

Table 3-47 presents I2C/I3C signal descriptions.

Table 3-47 I2C/I3C signal descriptions

Signal name	Type	Description	Ball location
I3C5			
SCL5	DIO	I3C5 serial clock	F5
SDA5	DIO	I3C5 serial data	F6
I3C6			

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Signal name	Type	Description	Ball location
SCL6	DIO	I3C1 serial clock	H7
SDA6	DIO	I3C1 serial data	G6
I2C0			
SCL0	DIO	I2C0 serial clock	Y4
SDA0	DIO	I2C0 serial data	W6
I2C1			
SCL1	DIO	I2C1 serial clock	M36
SDA1	DIO	I2C1 serial data	L36
I2C2			
SCL2	DIO	I2C2 serial clock	Y2
SDA2	DIO	I2C2 serial data	AA2
I2C3			
SCL3	DIO	I2C3 serial clock	W2
SDA3	DIO	I2C3 serial data	W1
I2C4			
SCL4	DIO	I2C4 serial clock	K36
SDA4	DIO	I2C4 serial data	K37

3.12.1.2 I2C Timing Characteristics

Table 3-48 and Figure 3-28 present timing characteristics for the I2C interfaces in SS/FS/FS+ modes.

Table 3-48 I2C timing characteristics (SS/FS/FS+ modes)

No.	Parameter		SS		FS		FS+		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
	t_c	Cycle time		10000		2500		1000	ns
IIC2	$t_{w\ high}$	Pulse duration, SCL high	4.0		0.6		0.26		µs
IIC3	$t_{w\ low}$	Pulse duration, SCL low	4.7		1.3		0.5		µs
IIC4	t_{RISE}	Rise time of SDA and SCL signals		1000	20	300		120	ns
IIC5	t_{FALL}(1)	Fall time of SDA and SCL signals		300	20 × (VDD/ 5.5V)	300	20 × (VDD/ 5.5V)	120	ns
IIC6	t_{su}	Setup time, SDA to SCL	250		100		50		ns
IIC7	t_h(2)	Hold time, SDA to SCL	5.0		0		0		µs
IIC8	$t_{su\ start}$	Setup time, SCL to repeated START (Sr) condition	4.7		0.6		0.26		µs
IIC9	$t_{h\ start}$	Hold time, START (S) condition to SCL	4.0		0.6		0.26		µs
IIC10	$t_{h\ stop}$	Setup time, SCL to STOP(P) condition	4.0		0.6		0.26		µs
IIC11	$t_{(BUF)}$	Bus free time between STOP (P) and START (S) condition	4.7		1.3		0.5		µs
IIC12	t_{DV}	Data valid time		3.45		0.9		0.45	µs
IIC13	t_{DV_ACK}	Data valid acknowledge time		3.45		0.9		0.45	µs

1. VDD: I2C IO voltage
2. I2C-bus devices

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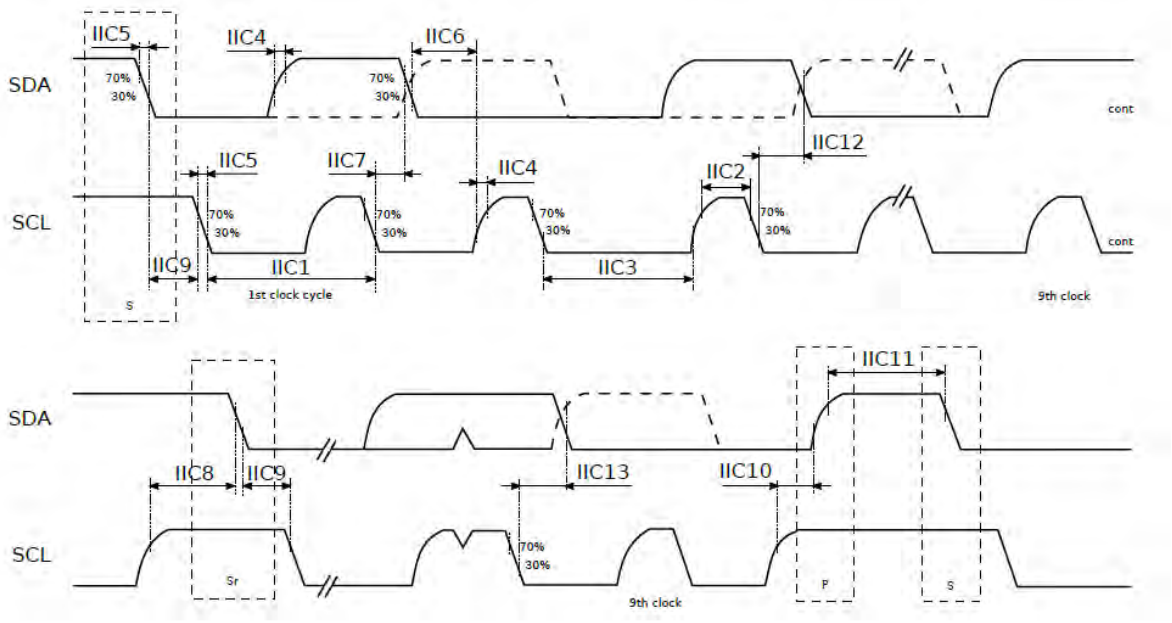

Figure 3-28 I2C timing diagram (SS/FS/FS+ modes)

Table 3-49 I2C timing characteristics (HS mode)

No.	Parameter		C_b=100pF (max)		C_b=400pF (max)		Unit
			Min.	Max.	Min.	Max.	
IIC1	t_c	Cycle time	0	294	0	588	ns
IIC2	$t_{su\ start}$	Setup time, SCL to repeated START condition	160		160		ns
IIC3	$t_{h\ start}$	Hold time, (repeated) START condition to SCL	160		160		ns
IIC4	$t_{w\ low}$	Pulse duration, SCL low	160		320		ns
IIC5	$t_{w\ high}$	Pulse duration, SCL high	60		120		ns
IIC6	t_h[(1)]	Hold time, SDA to SCL	0	70	0	150	ns
IIC7	t_{su}	Setup time, SDA to SCL	10		10		ns
IIC8	t_{RISE}	Rise time of SDA and SCL signals	10	40	20	80	ns
IIC9	t_{FALL}	Fall time of SDA and SCL signals	10	40	20	80	ns
IIC10	$t_{h\ stop}$	Setup time, SCL to STOP condition	160		160		ns

1. I2C-bus devices

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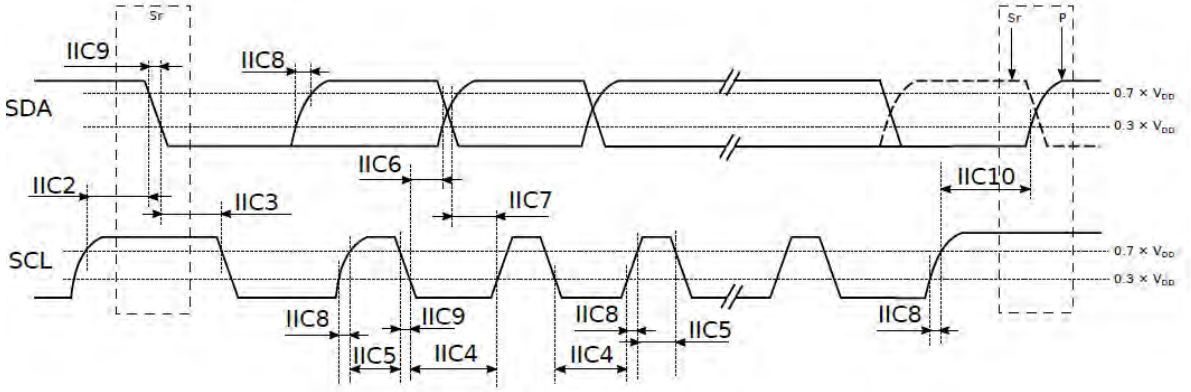

Figure 3-29 I2C timing diagram (HS mode)

3.12.2 Universal Asynchronous Receiver/Transmitter (UART)

The device supports four UART modules, which provide full-duplex serial communication with external devices. UART1 and UART2 are 4-pin channels (TX, RX, CTS, RTS) while UART0, and UART3 are 2-pin channels (TX, RX).

Each UART module supports the following key features:

- 16C450-compatible
- 16550A-compatible
- Transfer system: Asynchronous
- Configurable communication format:
  - 5, 6, 7, or 8 data bits
  - Optional parity bit
  - 1 or 2 stop bits
- Internal 16-bit programmable baud rate generator
- 8-bit scratch register
- Separate transmit and receive 32-byte FIFOs
- Programmable baud rates from 300 bps up to 3 Mbps
- Baud rate error less than 0.25%
- Two DMA handshake lines
- Internal diagnostic capabilities with loopback
- Polling, DMA, and interrupt modes of operation
- Hardware flow control (RTS/CTS)
- Software flow control (Xon/Xoff)

3.12.2.1 UART Signal Descriptions

Table 3-50 presents UART signal descriptions.

Table 3-50 UART signal descriptions

Signal name	Type	Description	Ball location
UART0			
URXD0	DI	UART0 receive data	U3
UTXD0	DO	UART0 transmit data	U2
UART1			

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Signal name	Type	Description	Ball location
URXD1	DI	UART1 receive data	U10, G3, V2, R33, AC6
UTXD1	DO	UART1 transmit data	Y10, G4, V1, R34, AA6
UCTS1	DI	UART1 clear to send (active low)	Y7, G5, U5, P31, AD10
URTS1	DO	UART1 request to send (active low)	Y6, E3, U4, T33, AD11
UART2			
URXD2	DI	UART2 receive data	U5, G1, P31, AB5
UTXD2	DO	UART2 transmit data	U4, G2, T33, AB6
UCTS2	DI	UART2 clear to send (active low)	V2, E2, R33, AA5
URTS2	DO	UART2 request to send (active low)	V1, F2, R34, AC5
UART3			
URXD3	DI	UART3 receive data	AA35, U8, R30, H32, AB1
UTXD3	DO	UART3 transmit data	AB32, U7, P32, G30, AB2

3.12.3 Serial Peripheral Interface (SPI)

3.12.3.1 SPI Master

The SPI Master (SPIM) is a synchronous serial interface that supports single mode (4-pin), dual mode (4-pin) and quad mode (6-pin) used for short-distance communication, primarily in embedded systems. The device features six SPIM controllers.

The SPIM supports the following key features:

- SPIM0 supports single/dual/quad mode up to 52 MHz, and only half duplex mode in quad mode
- SPIM[1-5] support single/dual mode up to 52 MHz, half and full duplex mode
- Two configurable transmit modes:
  - TX DMA mode—the SPI controller automatically fetches the transmitted data (to be put on the MOSI line) from memory
  - TX PIO mode—the data to be transmitted on the MOSI line is written to FIFO before the start of the transaction, the depth of the TX FIFO is 32 bytes.
- Two configurable receive modes:
  - RX DMA mode—the SPI controller automatically stores the received data (from MISO line) to memory.
  - RX PIO mode—the received data is kept in RX FIFO of the SPI controller. The processor must read back the data by itself, the depth of the RX FIFO is 32 bytes.
- Configurable chip-select setup, hold, and idle times
- Programmable serial clock high and low times
- Configurable transmit and receive bit order (MSB or LSB)
- Programmable byte length for transmission
- Unlimited length for transmission using dedicated pause mode
- Configurable option to control chip-select de-assertion between byte transfers
- Supports all clock polarity and phase modes
- CS GPIO Mode—expand chip select pin for connecting multi-SPI slave device by software configured GPIO

3.12.3.1.1 SPI Master Signal Descriptions

Table 3-51 presents SPIM signal descriptions.

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Table 3-51 SPIM signal descriptions

Signal name	Type	Description	Ball location
SPI0 Master			
SPIM0_CLK	DO	SPIM0 clock	T11
SPIM0_CSB	DO	SPIM0 chip select	V6
SPIM0_MISO	DIO	SPIM0 data in/SPIM0 data 1	V8
SPIM0_MOSI	DIO	SPIM0 data out/SPIM0 data 0	V7
SPIM0_MIO2	DIO	SPIM0 data 2	U7
SPIM0_MIO3	DIO	SPIM0 data 3	U8
SPI1 Master			
SPIM1_CLK	DO	SPIM1 clock	T10
SPIM1_CSB	DO	SPIM1 chip select	T9
SPIM1_MISO	DIO	SPIM1 data in/SPIM0 data 1	T7
SPIM1_MOSI	DIO	SPIM1 data out/SPIM0 data 0	T8
SPI2 Master			
SPIM2_CLK	DO	SPIM2 clock	G1
SPIM2_CSB	DO	SPIM2 chip select	G2
SPIM2_MISO	DIO	SPIM2 data in/SPIM0 data 1	E2
SPIM2_MOSI	DIO	SPIM2 data out/SPIM0 data 0	F2
SPI3 Master			
SPIM3_CLK	DO	SPIM3 clock	W5, AC6
SPIM3_CSB	DO	SPIM3 chip select	W4, AA6
SPIM3_MISO	DIO	SPIM3 data in/SPIM0 data 1	V5, AB4
SPIM3_MOSI	DIO	SPIM3 data out/SPIM0 data 0	V4, AC7
SPI4 Master			
SPIM4_CLK	DO	SPIM4 clock	T30, AC31
SPIM4_CSB	DO	SPIM4 chip select	R31, AD30
SPIM4_MISO	DIO	SPIM4 data in/SPIM0 data 1	U32, AB31
SPIM4_MOSI	DIO	SPIM4 data out/SPIM0 data 0	T31, AC30
SPI5 Master			
SPIM5_CLK	DO	SPIM5 clock	U10, AC9
SPIM5_CSB	DO	SPIM5 chip select	Y10, AB9
SPIM5_MISO	DIO	SPIM5 data in/SPIM0 data 1	Y7, AC4
SPIM5_MOSI	DIO	SPIM5 data out/SPIM0 data 0	Y6, AB8

3.12.3.1.2 SPI Master Timing Characteristics

Table 3-52 and Figure 3-30 present timing characteristics for the SPIM in the device.

Table 3-52 SPIM timing characteristics

No.	Parameter		Min.	Typ.	Max.	Unit
	f_{OP_MCK}	SPI clock frequency			52	MHz
SPI02	t_c	Cycle time, SPI clock (SPI_CLK)	19.23[(1)]			ns
SPI05	$t_{w\_CLK\_L}$	Pulse duration, SPI_CLK low	7.2			ns

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No.	Parameter		Min.	Typ.	Max.	Unit
SPI06	$t_{w\_CLK\_H}$	Pulse duration, SPI_CLK high	7.2			ns
SPI07	t_{su_cs}[4]	SPI_CSB falling to SPI_SCK rising setup time	1.8			ns
SPI08	t_{h_cs}[4]	SPI_SCK falling to SPI_CSB rising hold time	1.8			ns
SPI09	t_{su_MOSI}	SPI_MO to SPI_CK rising setup time	6.6			ns
SPI010	t_{h_MOSI}	SPI_SCK rising to SPI_MO hold time	6.6			ns
SPI011	t_{su_MISO}[2]	SPI_MI to _SPI SCK rising setup time requirement	0			ns
SPI012	t_{h_MISO}[3]	SPI_SCK rising to SPI_MI hold time requirement	0			ns

1. For maximum operating clock frequency refer to Table 6-1 Maximum performance ratings.
2. To achieve the minimum value of t_{su_MISO}, the internal sample clock delay of SPIM should be adjusted.
3. t_{h_MISO} data valid time should be one cycle of f_{OP_MCK}.
4. In CS GPIO mode, SPI_CSB is handled by SW. SW should pull down SPI_CSB pin before SPI starts transferring and pull up SPI_CSB pin when SPI completes the transaction.

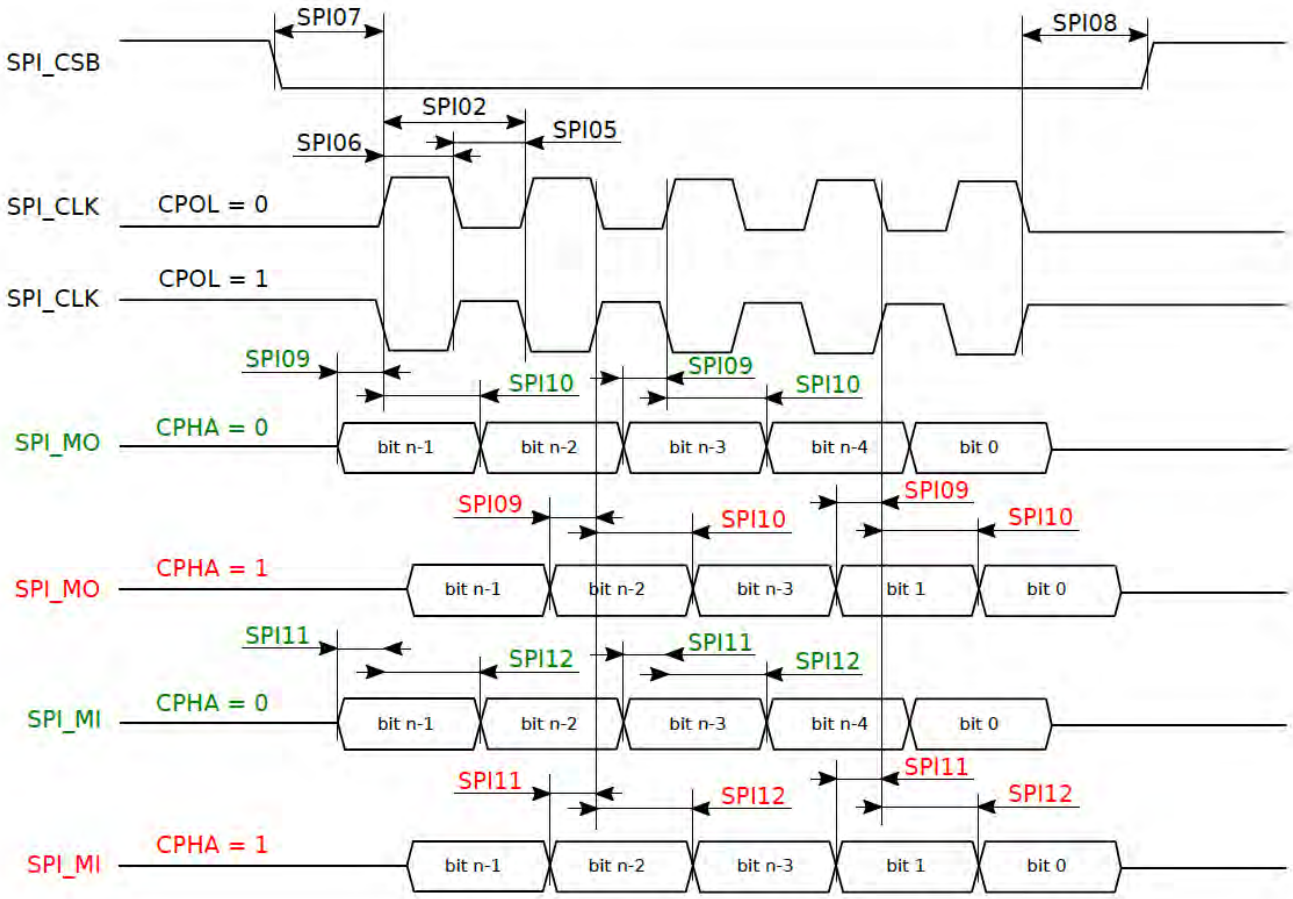

Figure 3-30 SPIM timing diagram

3.12.4 Universal Serial Bus (USB)

The device has three USB subsystems with integrated PHYs—one SuperSpeed (SS) USB 3.1 Gen1 DRD and two USB 2.0 Dual-Role-Device (DRD)

- USB Port 1 supports SS USB 3.1 Gen1 DRD.
- USB Port 0 and USB Port 2 are USB 2.0 DRD ports.

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The features of the USB subsystems include:

- USB 3.1 SS Gen1 with 5 Gbps TX and 5 Gbps RX (USB Port 1 only)
  - Embedded USB 3.1 Gen1 PHY with 32-bit @ 125 MHz PIPE interface
  - U0/U1/U2/U3 states
- USB 2.0 Full-Speed (FS) 12 Mbps and High-Speed (HS) 480 Mbps
  - Embedded USB 2.0 PHY with 16-bit @ 30 MHz UTMI+ interface
  - Lower Power Management (LPM)
- Host role features:
  - Host controller based on eXtensible Host Controller Interface (xHCI) Revision 1.1
  - Dedicated DMA channel for USB 3.1 data transfer
  - Support of all USB compliant data transfer types (Control/Bulk/Interrupt/Isochronous)
  - Support of connection to USB 2.0/USB 3.0 Hubs
  - Support of up to 15 devices
  - Support of up to 64 endpoints
- Device (peripheral) role features:
  - Proprietary application layer device controller
  - Embedded queue management function with scatter/gather DMA capability
  - Shared endpoint and buffer hardware for USB 2.0 and USB 3.1 Gen1 ports
  - Up to 8 OUT endpoints and 8 IN endpoints
  - Up to 8 packet slots for each endpoint
  - Software configurable FIFO size allocation for each endpoint
  - Software configurable transfer type (Bulk/Interrupt/Isochronous) for each endpoint
  - Software configurable interrupt with the following interrupt statuses: VBUS On/Off, suspend/resume, USB Reset
  - Software configurable period from VBUS connection to D+ pull-up
  - Data alignment for Device DMA descriptor: 16-Byte
  - Data alignment for Device data: Byte alignment

- USB20 PHY
  - Standard PHY UTM interface
  - Serial data transmission rates of 480 Mbps, 12 Mbps and 1.5 Mbps
  - Utilize 16-bit parallel interface to transmit and receive USB data
  - Clock and Data Recovery (CDR) from high-speed serial stream on the USB bus
  - NRZI encoding and decoding
  - Bit-stuffing and bit-unstuffing

- USB30 PHY
  - Standard PHY interface provides a target interface for USB SuperSpeed PHY vendors.
  - Support 5.0 GT/s serial data transmission rate
  - Utilize 32-bit parallel interface to transmit and receive USB SuperSpeed data
  - Allow integration of high speed components into a single functional block
  - Clock and Data Recovery (CDR) from serial stream on the USB SuperSpeed bus
  - Holding registers to stage transmit and receive data
  - Direct disparity control for use in transmitting compliance pattern(s)
  - 8-/10-bit encoding/decoding and error indication

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- Receiver detection
- Low Frequency Periodic Signaling (LFPS) Transmission
- Selectable TX Margining

3.12.4.1 USB Signal Descriptions

Table 3-53 presents USB signal descriptions.

Table 3-53 USB signal descriptions

Signal name	Type	Description	Ball location
USB Port 0			
USB_DP_P0	AIO	USB D+ bi-directional differential data	W32
USB_DM_P0	AIO	USB D- bi-directional differential data	W31
IDDIG	DI	USB OTG ID. Cable end detector: • GND: micro-A • Floating: micro-B	R36
USB_DRVVBUS	DO	USB drive VBUS—signal to external power switch enable	P36
VBUSVALID	DI	Digital VBUS—valid signal from external circuitry	P34
USB Port 1			
SSUSB_RXN	AI	USB SuperSpeed receive data negative	W36
SSUSB_RXP	AI	USB SuperSpeed receive data positive	W37
SSUSB_TXN	AO	USB SuperSpeed transmit data negative	Y34
SSUSB_TXP	AO	USB SuperSpeed transmit data positive	Y33
USB_DP_P1	AIO	USB D+ bi-directional differential data	U37
USB_DM_P1	AIO	USB D- bi-directional differential data	U36
VBUSVALID_1P	DI	Digital VBUS-valid signal from external circuitry	AC33, T33
IDDIG_1P	DI	USB OTG ID. Micro-A/B cable end detector	AB34, R34
USB_DRVVBUS_1P	DO	USB drive VBUS—signal to external power switch enable	AC32, R33
USB Port 2			
USB_DP_P2	AIO	USB D+ bi-directional differential data	V34
USB_DM_P2	AIO	USB D- bi-directional differential data	V35
VBUSVALID_2P	DI	Digital VBUS-valid signal from external circuitry	AB33, R30
IDDIG_2P	DI	USB OTG ID. Micro-A/B cable end detector	AD32, P31
USB_DRVVBUS_2P	DO	USB drive VBUS—signal to external power switch enable	AD33, P32

3.12.5 Ethernet Network Interface Controller (ENIC)

The device features one ENIC supporting the following key features:

- Compliance to standards:
  - MII/RMII/RGMII
  - IEEE 802.3-2015 for Ethernet MAC
  - IEEE 1588-2008 for precision networked clock synchronization
  - IEEE 802.1AS-2011 and 802.1-Qav-2009 for Audio Video (AV) traffic
  - IEEE 802.1Qbv-2015, 802.1Qbu-2016, and 802.1AS-Rev D5.0 for Time-Sensitive Networking (TSN) traffic
  - IEEE 802.3az-2010 for Energy Efficient Ethernet (EEE)

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- MAC features:
  - 10/100/1000 Mbps speed mode
  - Half-duplex operation:
    - Support of CSMA/CD protocol
    - Support of flow control using backpressure
  - Full-duplex flow control operation (IEEE 802.3x pause packets and priority flow control)
  - Support Ethernet packet timestamping as described in IEEE 1588-2002 and IEEE 1588-2008. Both one-step and two-step timestamping is supported in TX direction.
  - Flexibility to control the Pulse-Per-Second (PPS) output signal (ptp_pps_o)
  - Receive:
    - Automatic pad and CRC stripping options
    - Preamble and Start Frame Delimiter (SFD) deletion
    - Option to disable automatic CRC checking
    - Flexible address filtering modes:
      - Up to 31 additional 48-bit destination address filters with masks for each byte
      - Up to 31 × 48-bit source address comparison check with masks for each byte
      - 256-bit hash filter for multicast and unicast destination addresses
      - Option to pass all multicast addressed packets
      - Promiscuous mode to pass all packets without any filtering for network monitoring
    - Additional packet filtering:
      - VLAN tag-based: Perfect match and hash-based filtering. Filtering based on either outer or inner VLAN tag is possible.
      - Layer 3 and Layer 4-based: TCP or UDP over IPv4 or IPv6
      - Extended VLAN tag based with 4 filters selection
    - IEEE 802.1Q VLAN tag detection and option to delete the VLAN tags in received packets
    - Optional module to detect AMD magic packets
    - Optional forwarding of received pause packets to the application (in full-duplex mode)
    - Optional Receive module for Layer 3/Layer 4 checksum offload for received packets
    - Optional stripping of up to two VLAN Tags and providing the tags in the status
  - Transmit:
    - Automatic pad and CRC generation control ability on a per-packet basis
    - Preamble and start of packet data insertion
    - Programmable packet length to support standard or jumbo Ethernet packets of up to 16 KB
    - Programmable inter packet gap (40-bit to 96-bit times in steps of 8)
    - IEEE 802.3x flow control automatic transmission of zero-quanta pause packet when the flow control input transitions from assertion to de-assertion (in full-duplex mode)
    - Source address field insertion or replacement, and VLAN insertion, replacement, and deletion in transmitted packets with per-packet or static-global control
    - Insertion, replacement, or deletion of up to two queue/channel-based VLAN tags
- MAC Transaction Layer (MTL) features:
  - Receive:
    - 16KB RX FIFO and 4 RX queues
  - Transmit:
    - 16KB TX FIFO and 4 TX queues
    - Store-and-forward mechanism or threshold mode (cut-through) for transmission to the MAC

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- Calculate and insert IPv4 header checksum and TCP, UDP, or ICMP checksums
- Scheduling algorithms:
  - Weighted Round Robin (WRR)
  - Strict Priority (SP)
  - Credit-Based Shaper (CBS) when audio-video bridging is enabled

- Clause 22 and Clause 45 MDIO master interface for PHY configuration and management

3.12.5.1 ENIC Signal Descriptions

Table 3-54 presents ENIC signal descriptions.

Table 3-54 ENIC signal descriptions

Signal name	Type	Description	Ball location
ENIC Receive Data Bus—GBE_RXD[3:0]			
GBE_RXD0	DI	Gigabit Ethernet RX data 0	AB7
GBE_RXD1	DI	Gigabit Ethernet RX data 1	AC8
GBE_RXD2	DI	Gigabit Ethernet RX data 2	AA8
GBE_RXD3	DI	Gigabit Ethernet RX data 3	AB3
ENIC Transmit Data Bus—GBE_TXD[3:0]			
GBE_TXD0	DO	Gigabit Ethernet TX data 0	AC4
GBE_TXD1	DO	Gigabit Ethernet TX data 1	AB8
GBE_TXD2	DO	Gigabit Ethernet TX data 2	AC9
GBE_TXD3	DO	Gigabit Ethernet TX data 3	AB9
ENIC Command, Status, Clock and Interrupt Signals			
GBE_COL	DI	Gigabit Ethernet collision detected	AD11
GBE_INTR	DI	Gigabit Ethernet interrupt from external PHY	AD10
GBE_RXC	DI	Gigabit Ethernet RX clock	AB5
GBE_RXDV	DI	Gigabit Ethernet RX data valid	AC5
GBE_RXER	DI	Gigabit Ethernet RX error	AB4
GBE_TXC	DIO	Gigabit Ethernet TX clock	AB6
GBE_TXEN	DO	Gigabit Ethernet TX data valid	AA5
GBE_TXER	DO	Gigabit Ethernet TX error	AC7
ENIC Management Bus			
GBE_MDC	DO	Gigabit Ethernet MDC	AA6
GBE_MDIO	DIO	Gigabit Ethernet MDIO	AC6
Ethernet Auxiliary Snapshot and Pulse-Per-Second Signal			
GBE_AUX_PPS0	DIO	Ethernet Auxiliary Snapshot Input 0 / Pulse-Per-Second Output 0	AB2
GBE_AUX_PPS1	DIO	Ethernet Auxiliary Snapshot Input 1 / Pulse-Per-Second Output 1	AB1
GBE_AUX_PPS2	DIO	Ethernet Auxiliary Snapshot Input 2 / Pulse-Per-Second Output 2	AC7
GBE_AUX_PPS3	DIO	Ethernet Auxiliary Snapshot Input 3 / Pulse-Per-Second Output 3	AB4

3.12.5.2 ENIC Timing Characteristics

Table 3-55 and Figure 3-31 present timing characteristics for the ENIC MII in the device.

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Table 3-55 ENIC MII timing characteristics

No.	Parameter		Min.	Typ.	Max.	Unit
MII1	$t_{c\_TXC\_RXC}$	Cycle time, TXC/RXC		40		ns
MII2	t_{d_TX}	Delay time, transmission			9.764	ns
MII3	t_{d_TXC}	Delay time, TXC	1.323		2.273	ns
MII4	t_{d_TXD}	Delay time, TXD/TXEN/TXER	4.149		7.491	ns
MII5	t_{d_RXC}	Delay time, RXC	1.514		2.654	ns
MII6	t_{d_RXD}	Delay time, RXD/RXDV/RXER	2.041		4.021	ns
MII7	t_{su_RX}	Setup time, RXD/RXDV/RXER	3.507			ns
MII8	t_{h_RX}	Hold time, RXD/RXDV/RXER	0.473			ns
	D	Duty cycle, TXC/RXC 40 50 60 %	40	50	60	%
MII10	t_{RISE}	Rise time, TXC/RXC (20% ~ 80%)			0.75	ns
MII11	t_{FALL}	Fall time, TXC/RXC (20% ~ 80%)			0.75	ns

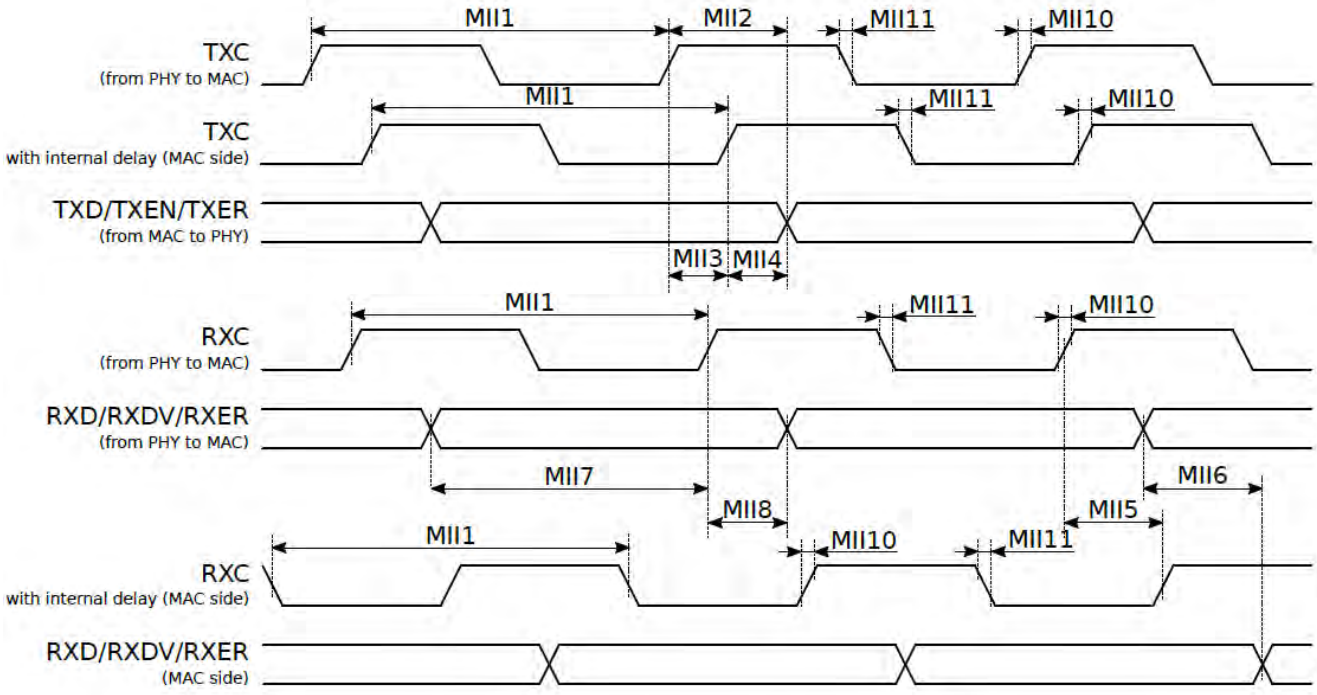

Figure 3-31 ENIC MII timing diagram

Table 3-56 and Figure 3-32 present timing characteristics for the ENIC RMII in the device.

Table 3-56 ENIC RMII timing characteristics

No.	Parameter		Min.	Typ.	Max.	Unit
RMII1	t_{c_REFCLK}	Cycle time, REFCLK		20		ns
RMII2	t_{d_TX}	Delay time, transmission			7.235	ns
RMII3	t_{d_TXC}	Delay time, REFCLK (when transmitting)	1.144		2.2	ns
RMII4	t_{d_TXD}	Delay time, TXD/TXEN	2.8		5.035	ns
RMII5	t_{d_RXC}	Delay time, REFCLK (when receiving)	1.798		3.071	ns
RMII6	t_{d_RXD}	Delay time, RXD/RXDV	1.925		3.469	ns
RMII7	t_{su_RX}	Setup time, RXD/RXDV	2.671			ns

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No.	Parameter		Min.	Typ.	Max.	Unit
RMII8	t_{h_RX}	Hold time, RXD/RXDV	0.873			ns
	D	Duty cycle, REFCLK	45	50	55	%
RMII10	t_{RISE}	Rise time, REFCLK (20% ~ 80%)			0.75	ns
RMII11	t_{FALL}	Fall time, REFCLK (20% ~ 80%)			0.75	ns

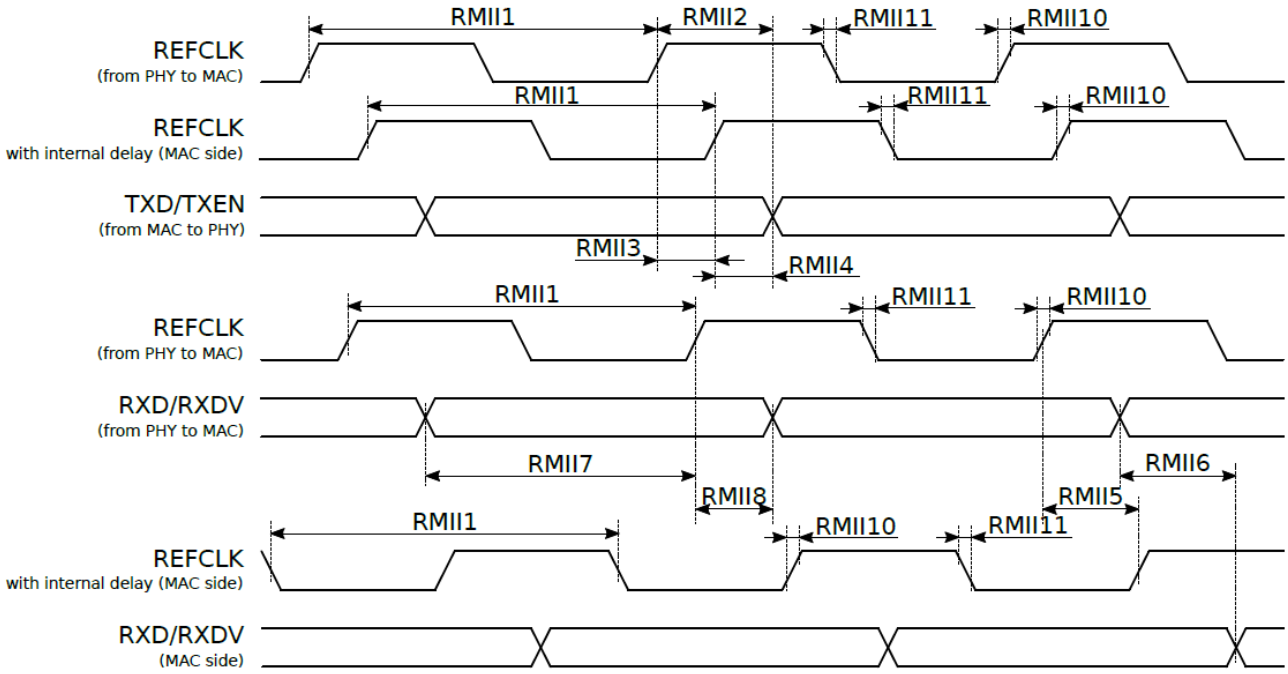

Figure 3-32 ENIC RMII timing diagram

Table 3-57 and Figure 3-33 present timing characteristics for the ENIC RGMII in the device.

Table 3-57 ENIC RGMII timing characteristics

No.	Parameter		Min.	Typ.	Max.	Unit
RGMII1	t_{TXC_RXC}	Cycle time, TXC/RXC (10M/100M/1000M)		400/40/8		ns
RGMII2	t_{d_TX}	Delay time, transmission			4.1 + K[(1)]	ns
RGMII3	t_{d_TXC}	Delay time, TXC	3.489		8.169	ns
RGMII4	t_{d_TXD}	Delay time, TXD/TX_CTL	4.141		7.491	ns
RGMII5	t_{d_RXC}	Delay time, RXC	1.998		3.575	ns
RGMII6	t_{d_RXD}	Delay time, RXD/RX_CTL	1.913		3.548	ns
RGMII7	t_{su_RX}	Setup time, RXD/RX_CTL	2.55 - Q[(2)]			ns
RGMII8	t_{h_RX}	Hold time, RXD/RX_CTL	1.085 + Q[(2)]			ns
	D	Duty cycle, TXC/RXC (1000M)	45	50	55	%
		Duty cycle, TXC/RXC (10M/100M)	40	50	60	%
RGMII10	t_{RISE}	Rise time, REFCLK (20% ~ 80%)			0.75	ns
RGMII11	t_{FALL}	Fall time, REFCLK (20% ~ 80%)			0.75	ns

1. K is programmable MAC internal delay (32-levels). The maximum delay is from 12.6001 ns to 28.5724 ns.
2. Q is programmable MAC internal delay (32-levels). The maximum delay is from 12.6001 ns to 28.5724 ns.

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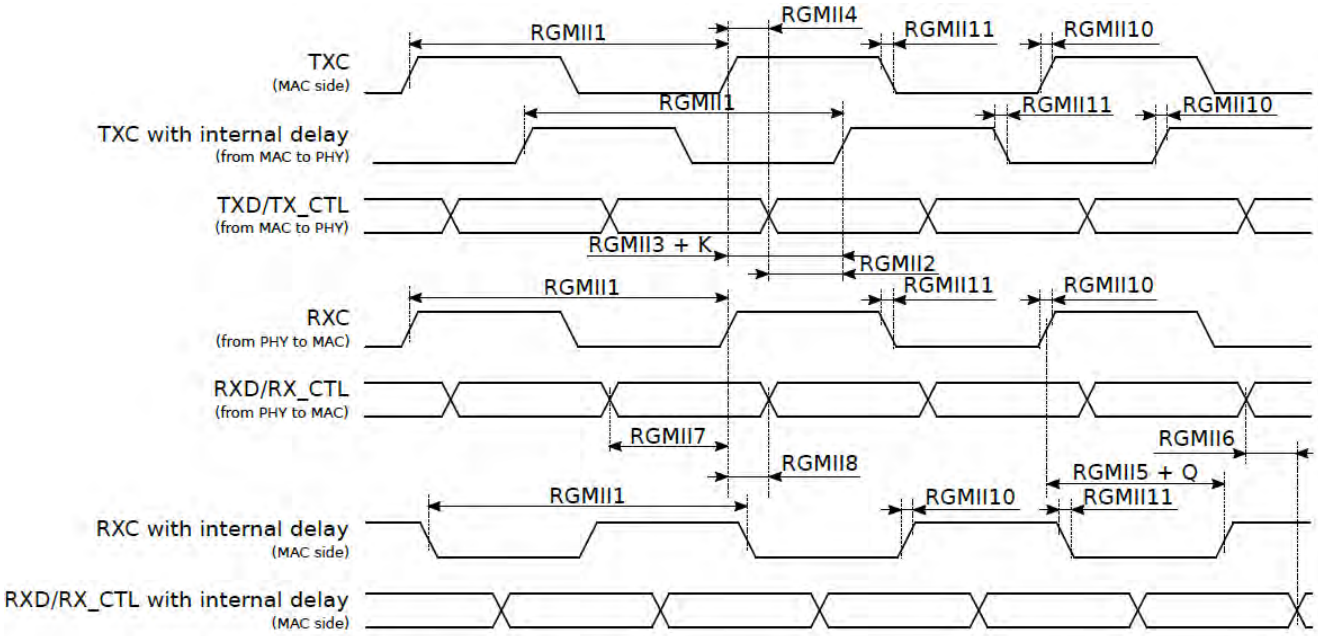

Figure 3-33 ENIC RGMII timing diagram

Table 3-58 and Figure 3-34 present timing characteristics for the ENIC MDIO in the device.

Table 3-58 ENIC MDIO timing characteristics

No.	Parameter		Min.	Typ.	Max.	Unit
MDIO1	t_{c_MDC}	Cycle time, MDC	400			ns
MDIO2	t_{d_MDO}	Delay time, MDIO output		MDIO4 - MDIO3		ns
MDIO3	t_{d_MDC}	Delay time, MDC	3.631		9.043	ns
MDIO4	$t_{d\_MDO\_MAC}$	Delay time, MDIO output (MAC to PHY)	4.804		11.479	ns
MDIO5	t_{d_MDI}	Delay time, MDIO input	1.92		4.203	ns
MDIO6	t_{su_MDI}	Setup time, MDIO input	1 + MDIO5 + MDIO3			ns
MDIO7	t_{h_MDI}	Hold time, MDIO input	1 - MDIO5 - MDIO3			ns

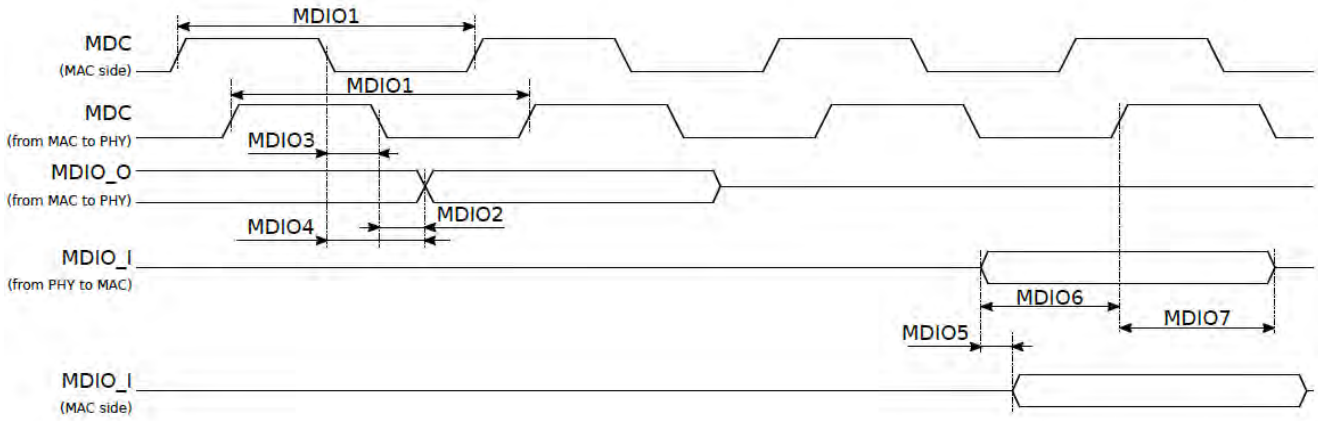

Figure 3-34 ENIC MDIO timing diagram

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3.12.6 Peripheral Component Interconnect Express (PCIe) Controller

The device features one Peripheral Component Interconnect Express (PCIe®) Controller that supports the following key features:

- One Port
- Compliant with the Intel® Physical Interface for PCI Express (PIPE) interface, allowing integration with PIPE-compliant PHY
- AMBA AXI4 specification compliant
- PCIe interface:
  - Mode: Root Complex (RC)
  - Link width: x1
  - Per lane link rate: 2.5 GT/s (Gen1) and 5.0 GT/s (Gen2)
  - PCI Express Base Specification Revision 2.0 compliant
  - PIPE 4.0 compliant
  - Memory transactions support
    - Maximum memory read request of 256 bytes
    - Maximum memory write request of 256 bytes
    - 32-bit addressing
  - I/O transactions:
    - Maximum I/O read request of 4 bytes
    - Maximum I/O write request of 4 bytes
    - 32-bit addressing
  - Configuration transactions:
    - Maximum configuration read request of 4 bytes
    - Maximum configuration write request of 4 bytes
    - Extended register number support (4 KB extended PCIe configuration header space)
  - Message transactions:
    - INTx interrupt signaling
    - Power management
    - Error signaling
    - Slot power limit
    - Vendor-defined messages
    - Latency Tolerance Reporting (LTR) message
  - One Virtual Channel (VC)
  - One physical function
  - Advanced Error Reporting (AER)
  - Endpoint Cyclic Redundancy Check (ECRC) generation and check
  - Lane reversal
  - Polarity inverse support
  - Legacy PCI power management support
  - Active State Power Management (ASPM) L0s and L1 state support
  - L1 Power Management Substates (L1PMSS) with CLKREQ# support
  - Message Signaled Interrupt (MSI), per function up to 32
- AHB and AXI interfaces:
  - One AHB slave interface for bridge configuration

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- One AXI master interface supporting up to 12/10 outstanding write/read requests
- One AXI slave interface supporting up to 6/4 outstanding write/read requests
- 128-bit data support for AXI master and slave interfaces

3.12.6.1 PCIe Signal Descriptions

Table 3-59 presents PCIe signal descriptions.

Table 3-59 PCIe signal descriptions

Signal name	Type	Description	Ball location
PCIe Control Signals Port			
PERSTN	DO	Fundamental reset	AA3, AA8
CLKREQN	DIO	Clock request	AA1, AC8
WAKEN	DI	Link reactivation	AA4, AB3
PCIe Port			
PCIE_CKN(1)	AI	Reference clock differential pair	AN3
PCIE_CKP(1)	AI		AN4
PCIE_LN0_RXN	AI	Lane 0 receive data differential pair	AP1
PCIE_LN0_RXP	AI		AP2
PCIE_LN0_TXN	AO	Lane 0 transmit data differential pair	AM2
PCIE_LN0_TXP	AO		AM1

1. Connect this pin through an external 49.9 Ω (1%) resistor to GND.

3.12.7 KeyPad Scanner (KeyPad)

The KeyPad module implements scanning algorithm for hardware-based key-press decoding.

The KeyPad supports the following key features:

- Type of keyboards: 2 × 2 single key
- Key detection block providing key pressed, key released and de-bounce mechanisms
- Interrupt event detection on pressed and released keys
- Detection of one or two keys pressed simultaneously with any combination

3.12.7.1 KeyPad Signal Descriptions

Table 3-60 presents KeyPad signal descriptions.

Table 3-60 KeyPad signal descriptions

Signal name	Type	Description	Ball location
KPCOL0	DIO	KeyPad column 0	H31
KPCOL1	DIO	KeyPad column 1	J31
KPROW0	DIO	KeyPad row 0	J30
KPROW1	DIO	KeyPad row 1	K30

3.12.8 General-Purpose I/O (GPIO)

The GPIO peripheral provides 177 dedicated GPIO pins, multiplexed with other functions to reduce the pin count.

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Each GPIO pin has the following key functions:

- Configurable direction: input or output
- Control of the state driven on the output pin when GPIO is configured as an output
- Detection of the state of the pin when GPIO is configured as an input
- Configurable interrupt event generation

3.12.8.1 GPIO Signal Descriptions

Table 3-61 presents GPIO signal descriptions.

Table 3-61 GPIO signal descriptions

Signal name	Type	Description	Ball location
GPIO0	DIO	General-purpose input and output	Y10
GPIO1	DIO	General-purpose input and output	U10
GPIO2	DIO	General-purpose input and output	Y6
GPIO3	DIO	General-purpose input and output	Y7
GPIO4	DIO	General-purpose input and output	Y8
GPIO5	DIO	General-purpose input and output	W7
GPIO6	DIO	General-purpose input and output	W3
GPIO7	DIO	General-purpose input and output	W4
GPIO8	DIO	General-purpose input and output	W5
GPIO9	DIO	General-purpose input and output	V4
GPIO10	DIO	General-purpose input and output	V5
GPIO11	DIO	General-purpose input and output	W8
GPIO12	DIO	General-purpose input and output	R31
GPIO13	DIO	General-purpose input and output	T30
GPIO14	DIO	General-purpose input and output	T31
GPIO15	DIO	General-purpose input and output	U32
GPIO16	DIO	General-purpose input and output	AB32
GPIO17	DIO	General-purpose input and output	AA35
GPIO18	DIO	General-purpose input and output	G4
GPIO19	DIO	General-purpose input and output	G3
GPIO20	DIO	General-purpose input and output	E3
GPIO21	DIO	General-purpose input and output	G5
GPIO22	DIO	General-purpose input and output	E4
GPIO23	DIO	General-purpose input and output	E5
GPIO24	DIO	General-purpose input and output	F4
GPIO25	DIO	General-purpose input and output	Y9
GPIO26	DIO	General-purpose input and output	AA7
GPIO27	DIO	General-purpose input and output	AA11
GPIO28	DIO	General-purpose input and output	Y5
GPIO29	DIO	General-purpose input and output	AA9
GPIO30	DIO	General-purpose input and output	Y11
GPIO31	DIO	General-purpose input and output	U2
GPIO32	DIO	General-purpose input and output	U3

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Signal name	Type	Description	Ball location
GPIO33	DIO	General-purpose input and output	V1
GPIO34	DIO	General-purpose input and output	V2
GPIO35	DIO	General-purpose input and output	U4
GPIO36	DIO	General-purpose input and output	U5
GPIO37	DIO	General-purpose input and output	T6
GPIO38	DIO	General-purpose input and output	T5
GPIO39	DIO	General-purpose input and output	T4
GPIO40	DIO	General-purpose input and output	T1
GPIO41	DIO	General-purpose input and output	T2
GPIO42	DIO	General-purpose input and output	H31
GPIO43	DIO	General-purpose input and output	J31
GPIO44	DIO	General-purpose input and output	J30
GPIO45	DIO	General-purpose input and output	K30
GPIO46	DIO	General-purpose input and output	AB33
GPIO47	DIO	General-purpose input and output	AA4
GPIO48	DIO	General-purpose input and output	AA3
GPIO49	DIO	General-purpose input and output	AA1
GPIO50	DIO	General-purpose input and output	AB34
GPIO51	DIO	General-purpose input and output	AC32
GPIO52	DIO	General-purpose input and output	AC33
GPIO53	DIO	General-purpose input and output	AD32
GPIO54	DIO	General-purpose input and output	AD33
GPIO55	DIO	General-purpose input and output	Y4
GPIO56	DIO	General-purpose input and output	W6
GPIO57	DIO	General-purpose input and output	M36
GPIO58	DIO	General-purpose input and output	L36
GPIO59	DIO	General-purpose input and output	Y2
GPIO60	DIO	General-purpose input and output	AA2
GPIO61	DIO	General-purpose input and output	W2
GPIO62	DIO	General-purpose input and output	W1
GPIO63	DIO	General-purpose input and output	K36
GPIO64	DIO	General-purpose input and output	K37
GPIO65	DIO	General-purpose input and output	F5
GPIO66	DIO	General-purpose input and output	F6
GPIO67	DIO	General-purpose input and output	H7
GPIO68	DIO	General-purpose input and output	G6
GPIO69	DIO	General-purpose input and output	V6
GPIO70	DIO	General-purpose input and output	T11
GPIO71	DIO	General-purpose input and output	V7
GPIO72	DIO	General-purpose input and output	V8
GPIO73	DIO	General-purpose input and output	U7
GPIO74	DIO	General-purpose input and output	U8
GPIO75	DIO	General-purpose input and output	T9

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Signal name	Type	Description	Ball location
GPIO76	DIO	General-purpose input and output	T10
GPIO77	DIO	General-purpose input and output	T8
GPIO78	DIO	General-purpose input and output	T7
GPIO79	DIO	General-purpose input and output	G2
GPIO80	DIO	General-purpose input and output	G1
GPIO81	DIO	General-purpose input and output	F2
GPIO82	DIO	General-purpose input and output	E2
GPIO83	DIO	General-purpose input and output	R36
GPIO84	DIO	General-purpose input and output	P36
GPIO85	DIO	General-purpose input and output	P34
GPIO86	DIO	General-purpose input and output	R34
GPIO87	DIO	General-purpose input and output	R33
GPIO88	DIO	General-purpose input and output	T33
GPIO89	DIO	General-purpose input and output	P31
GPIO90	DIO	General-purpose input and output	P32
GPIO91	DIO	General-purpose input and output	R30
GPIO92	DIO	General-purpose input and output	K32
GPIO93	DIO	General-purpose input and output	K31
GPIO94	DIO	General-purpose input and output	L30
GPIO95	DIO	General-purpose input and output	L31
GPIO96	DIO	General-purpose input and output	L33
GPIO97	DIO	General-purpose input and output	L34
GPIO98	DIO	General-purpose input and output	M31
GPIO99	DIO	General-purpose input and output	N37
GPIO100	DIO	General-purpose input and output	K34
GPIO101	DIO	General-purpose input and output	M33
GPIO102	DIO	General-purpose input and output	M35
GPIO103	DIO	General-purpose input and output	M34
GPIO104	DIO	General-purpose input and output	N33
GPIO105	DIO	General-purpose input and output	M30
GPIO106	DIO	General-purpose input and output	M32
GPIO107	DIO	General-purpose input and output	G36
GPIO108	DIO	General-purpose input and output	H36
GPIO109	DIO	General-purpose input and output	J36
GPIO110	DIO	General-purpose input and output	J37
GPIO111	DIO	General-purpose input and output	G33
GPIO112	DIO	General-purpose input and output	G32
GPIO113	DIO	General-purpose input and output	H35
GPIO114	DIO	General-purpose input and output	H34
GPIO115	DIO	General-purpose input and output	H33
GPIO116	DIO	General-purpose input and output	J34
GPIO117	DIO	General-purpose input and output	J33
GPIO118	DIO	General-purpose input and output	G31

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Signal name	Type	Description	Ball location
GPIO119	DIO	General-purpose input and output	G30
GPIO120	DIO	General-purpose input and output	H32
GPIO121	DIO	General-purpose input and output	AD30
GPIO122	DIO	General-purpose input and output	AC31
GPIO123	DIO	General-purpose input and output	AC30
GPIO124	DIO	General-purpose input and output	AB31
GPIO125	DIO	General-purpose input and output	N30
GPIO126	DIO	General-purpose input and output	N31
GPIO127	DIO	General-purpose input and output	P30
GPIO128	DIO	General-purpose input and output	N34
GPIO129	DIO	General-purpose input and output	P33
GPIO130	DIO	General-purpose input and output	P35
GPIO131	DIO	General-purpose input and output	AB9
GPIO132	DIO	General-purpose input and output	AC9
GPIO133	DIO	General-purpose input and output	AB8
GPIO134	DIO	General-purpose input and output	AC4
GPIO135	DIO	General-purpose input and output	AB3
GPIO136	DIO	General-purpose input and output	AA8
GPIO137	DIO	General-purpose input and output	AC8
GPIO138	DIO	General-purpose input and output	AB7
GPIO139	DIO	General-purpose input and output	AB6
GPIO140	DIO	General-purpose input and output	AB5
GPIO141	DIO	General-purpose input and output	AC5
GPIO142	DIO	General-purpose input and output	AA5
GPIO143	DIO	General-purpose input and output	AA6
GPIO144	DIO	General-purpose input and output	AC6
GPIO145	DIO	General-purpose input and output	AC7
GPIO146	DIO	General-purpose input and output	AB4
GPIO147	DIO	General-purpose input and output	AD11
GPIO148	DIO	General-purpose input and output	AD10
GPIO149	DIO	General-purpose input and output	AB2
GPIO150	DIO	General-purpose input and output	AB1
GPIO151	DIO	General-purpose input and output	D37
GPIO152	DIO	General-purpose input and output	E36
GPIO153	DIO	General-purpose input and output	F37
GPIO154	DIO	General-purpose input and output	D35
GPIO155	DIO	General-purpose input and output	E34
GPIO156	DIO	General-purpose input and output	F33
GPIO157	DIO	General-purpose input and output	F32
GPIO158	DIO	General-purpose input and output	E32
GPIO159	DIO	General-purpose input and output	D36
GPIO160	DIO	General-purpose input and output	F36
GPIO161	DIO	General-purpose input and output	D33

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Signal name	Type	Description	Ball location
GPIO162	DIO	General-purpose input and output	E35
GPIO163	DIO	General-purpose input and output	D3
GPIO164	DIO	General-purpose input and output	D4
GPIO165	DIO	General-purpose input and output	D2
GPIO166	DIO	General-purpose input and output	D1
GPIO167	DIO	General-purpose input and output	C4
GPIO168	DIO	General-purpose input and output	C3
GPIO169	DIO	General-purpose input and output	AC35
GPIO170	DIO	General-purpose input and output	AD35
GPIO171	DIO	General-purpose input and output	AD37
GPIO172	DIO	General-purpose input and output	AD36
GPIO173	DIO	General-purpose input and output	AB37
GPIO174	DIO	General-purpose input and output	AB35
GPIO175	DIO	General-purpose input and output	K33
GPIO176	DIO	General-purpose input and output	K35

3.12.9 Pulse Width Modulation (PWM)

The device features four generic PWM modules to generate pulse sequences with programmable frequency and duration for a variety of applications.

Each PWM module supports the following key features:

- Old mode
- FIFO mode
- Periodical memory and random modes

3.12.9.1 PWM Signal Descriptions

Table 3-62 presents PWM signal descriptions.

Table 3-62 PWM signal descriptions

Signal name	Type	Description	Ball location
PWM_0	DO	PWM output 0	V4, AB33, AC8, C4
PWM_1	DO	PWM output 1	V5, Y11, AA5, C3
PWM_2	DO	PWM output 2	E5, AA11, R34, AB5
PWM_3	DO	PWM output 3	F4, Y5, R33, AC5

3.12.9.2 PWM Output Frequency and Duty Cycle

Table 3-63 PWM output frequency and duty cycle [1]

Mode	Duty cycle	Output frequency
Old mode	(PWM_THRESH + 1) / (PWM_DATA_WIDTH + 1)	SRCLK / [CLK_DIV × (PWM_DATA_WIDTH + 1)]

1. BCLK can be selected as 26 MHz or 78 MHz by PWM_CK_26M_SEL.

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3.13 Misc

3.13.1 Timers and Counters

3.13.1.1 System Timer (SYSTMR)

The SYSTMR is a 64-bit, always-on, up-counter used as an universal timer in the device. The counter value of SYSTMR is passed to the application cores (A78 and A55), SCP, GPU, and other processors to provide uniform system timestamps for operating systems like Android™, Linux®, and RTOS.

The SYSTMR supports the following key features:

- Enabled by default to tick with 13 MHz clock period
- HW counter incremented compensation when switching to 32 kHz clock source
- 4 x 32-bit counter timeout value (read as 32-bit down counter)
- Security access permission control for each control register (with one-time lock bit)

3.13.1.2 General-Purpose Timer (GPT)

The device has one GPT module that includes five 32-bit and one 64-bit timers. Each GPT can operate on one of the two clock sources, RTC clock (32.768 kHz) or system clock (13 MHz).

Each GPT supports:

- ONE-SHOT mode
- REPEAT mode
- KEEP-GO mode
- FREERUN mode

3.13.1.3 Watchdog Timer (WDT)

The WDT module is a part of TOPRGU. For more information refer to Section 5.5 Reset.

3.13.2 Auxiliary Analog-to-Digital Converter (AUXADC)

The device features one AUXADC module. It is used to identify the plugged peripherals and perform temperature/voltage measurements.

The AUXADC module key features are:

- 12-bit Successive Approximation Register (SAR) ADC architecture
- 6 input channels operating in immediate mode
- Configurable auto-sampling function per channel
- Sequential channel serving from high to low channel
- Immediate analog-digital conversion with auto-set option
- Background detection and interrupt
- Temperature/voltage measurement

3.13.2.1 AUXADC Timing and Functional Characteristics

Table 3-64 presents timing and functional characteristics for AUXADC in the device.

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Table 3-64 AUXADC specifications

Parameter		Min.	Typ.	Max.	Unit
f_{OP}	Operating frequency		3.25		MHz
N	Resolution		12		Bit
f_S	Sampling rate at N-bit		3.25/(N+8)		MSPS
IN_{SW}	Input swing	0.05		1.45	V
C_{IN}	Input capacitance unselected channel		50		fF
	Input capacitance selected channel		4		pF
R_{IN}	Input resistance unselected channel		400		MΩ
$F_{cycle\_latency}$	Cycle latency		N+8		$1/f_{OP}$
D_{NL}	Differential non-linearity		+1.0/-1.0		LSB
I_{NL}	Integral non-linearity		+2.0/-2.0		LSB
SNR+D	Signal to noise and distortion ratio (1 kHz full swing input; 1.0833 MHz clock rate)	60	67		dB
I_{cc}	Current consumption during power-up		450		µA
	Current consumption during power-down		4		µA

3.13.3 Thermal Control Subsystem (TCSYS)

The device Thermal Control Subsystem (TCSYS) is based on several temperature sensors in the hot spots on the die. The thermal control module executes periodic measurements for each hot spot. The temperature readings are readable by software. In order to minimize the software effort to monitor temperature, the thermal controller generates interrupts to inform microprocessors of any abnormal condition.

The TCSYS supports the following key features:

- 6 banks with up to four thermal sensors
- Programmable periodic temperature measurement
- Two independent Finite State Machines (FSM) for temperature monitoring
- Different types of low pass filters for thermal sensor reading

The TCSYS has three major building blocks:

- Sensing device: Thermal Sensing Micro Circuit Unit (TSMCU)
- Converter: Low Voltage Thermal Sensor (LVTS) converter
- Digital Controller: LVTS_CTRL

Figure 3-35 shows the TCSYS top level block diagram.

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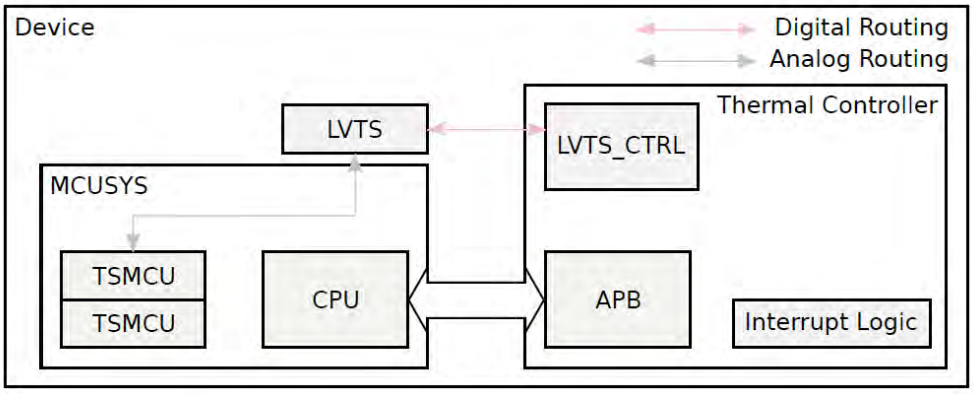

Figure 3-35 Thermal control subsystem

Table 3-65 presents the temperature sensors monitoring locations.

Table 3-65 Temperature sensor monitoring locations

Module	Sensor
A78	0, 1
A55	0, 1, 2, 3
APU	1
GPU + SoC	0 (GPU), 1 (GPU), 2 (SOC)
SoC	0, 1
ISP	0, 1

3.13.3.1 TCSYS Signal Descriptions

Table 3-66 presents TCSYS signal descriptions.

Table 3-66 TCSYS signal descriptions

Signal name	Type	Description	Ball location
LVTS_26M	DI	LVTS supported 26 MHz input frequency	AD37, P30
LVTS_FOUT	DO	LVTS output clock frequency	N30, AC35
LVTS_SCF	DI	LVTS serial clock frequency	N34, AD36
LVTS_SCK	DI	LVTS serial clock	P33, AB37
LVTS_SDI	DI	LVTS data input	P35, AB35
LVTS_SDO	DO	LVTS data output	AD35, N31

3.14 Boot Flash

The device supports the following boot flash:

- eMMC
- SPI NOR

Table 3-67 presents the boot flash selection options.

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Table 3-67 Boot flash selection

AUD_SYNC_MOSI	Boot flash
0	eMMC (default)
1	SPI NOR

3.15 ROM Power Down Mode

After system boot, ROM can be powered down and prevented from any probe of ROM content.

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4 Ball Map

Figure 4-1 presents simplified diagram of the location of the balls on the package.

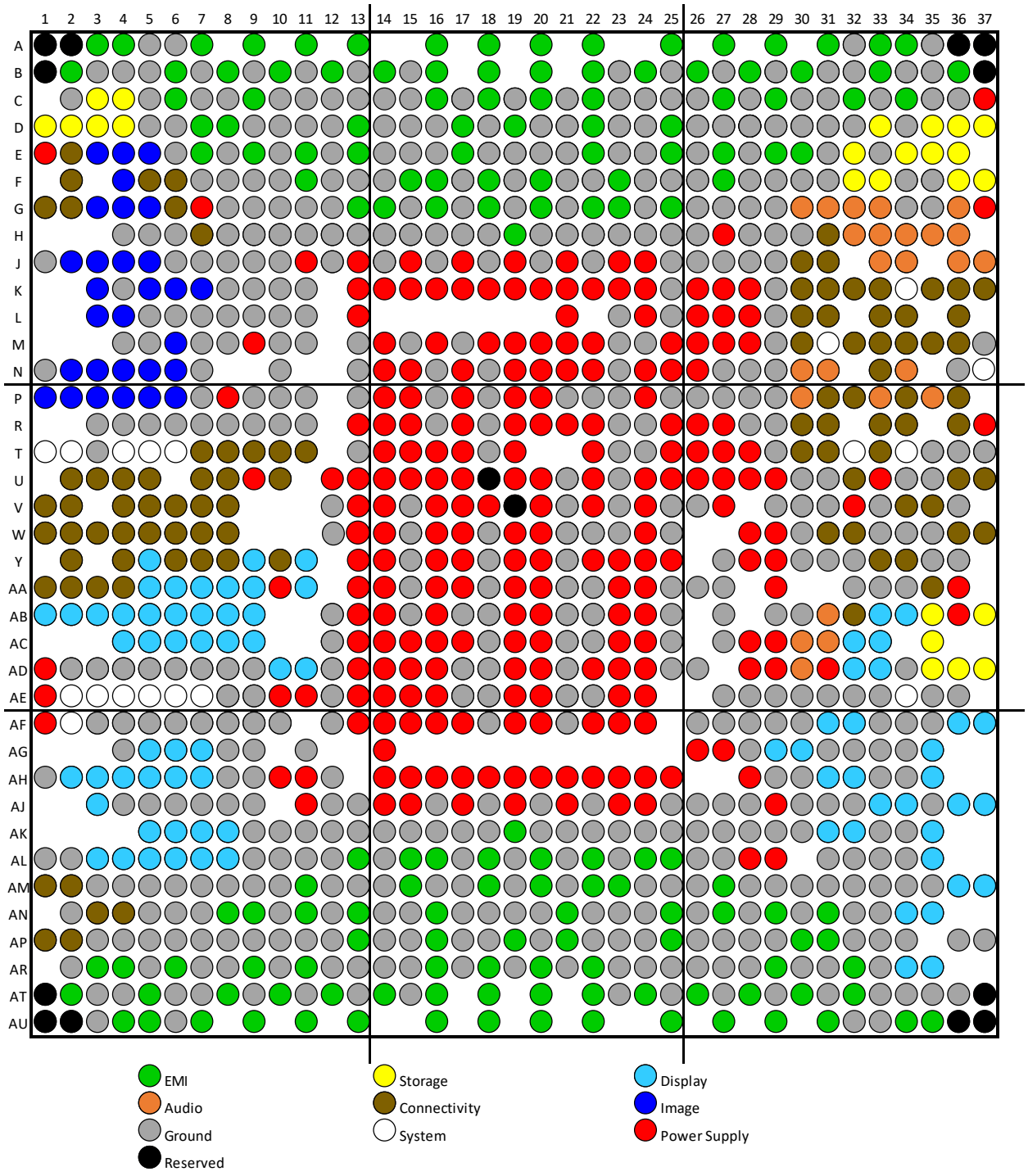

Figure 4-1 Ball map diagram

For detailed information about package outlines, thermal characteristics, and markings, see Section 7 Package Information.

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4.1 Quadrant Pinout

Figure 4-2 shows a top view mapping of the package quadrants.

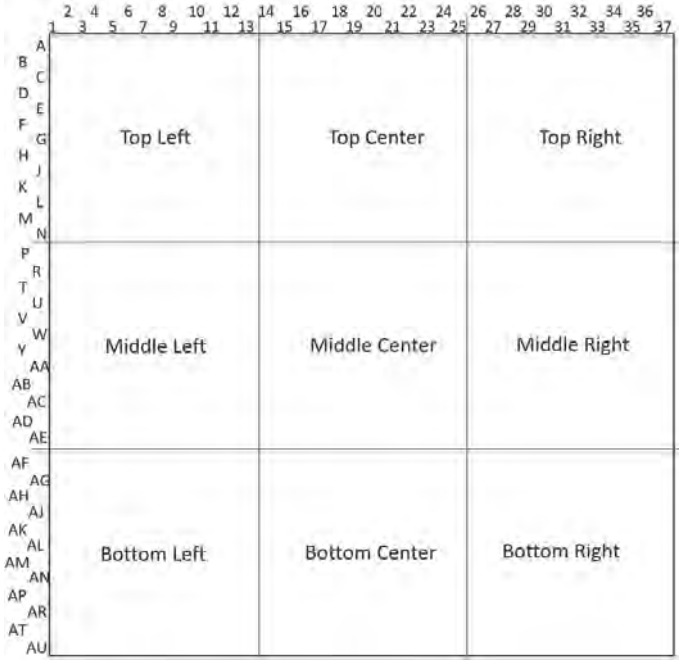

Figure 4-2 Package quadrants mapping

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4.1.1 LPDDR4(X)

Table 4-1 shows pin mapping on the top left part of the package.

Table 4-1 Ball map-top left

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	DUMMY	DUMMY	EMI2_TP	EMI2_DQ8	DVSS	DVSS	EMI2_DMI1		EMI2_DQ15		EMI2_DQ0		EMI2_DMI0
B	DUMMY	EMI2_EXTR	DVSS	DVSS	DVSS	EMI2_DQS1_T	DVSS	EMI2_DQ14	DVSS	EMI2_DQ7	DVSS	EMI2_DQ1	DVSS
C		DVSS	MSDC1_DAT3	MSDC1_DAT2	DVSS	EMI2_DQS1_C	DVSS	DVSS	EMI2_DQ12	DVSS	DVSS	DVSS	DVSS
D	MSDC1_DAT1	MSDC1_DAT0	MSDC1_CMD	MSDC1_CLK	DVSS	DVSS	EMI2_DQ13	EMI2_DQ10	DVSS	DVSS	DVSS	DVSS	EMI2_DQ3
E	DVDD18_MSDC1	SPIM2_MISO	CMMPDN1	CMMCLK0	CMMCLK1	DVSS	EMI2_DQ9	DVSS	EMI2_DQ11	DVSS	EMI2_DQS0_C	DVSS	EMI2_DQ5
F		SPIM2_MOSI		CMMCLK2	SCL5	SDA5	DVSS	DVSS	DVSS	DVSS	EMI2_DQS0_T	DVSS	DVSS
G	SPIM2_CLK	SPIM2_CSB	CMMRST0	CMMPDN0	CMMRST1	SDA6	DVDD28_MSDC1	DVSS	DVSS	DVSS	DVSS	DVSS	EMI2_DQ2
H				DVSS	DVSS	DVSS	SCL6	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS
J	DVSS	CSI1A_L1P_T0C	CSI1A_L1N_T1A	CSI1A_L0N_T0B	CSI1A_L0P_T0A	DVSS	DVSS	DVSS	DVSS	DVSS	DVDD18_IORT	DVSS	AVDD12_EMI2
K			CSI1B_L0N_T0B	DVSS	CSI1B_L0P_T0A	CSI1A_L2N_T1C	CSI1A_L2P_T1B	DVSS	DVSS	DVSS	DVSS		AVDD075_EMI2
L			CSI1B_L1P_T0C	CSI1B_L1N_T1A	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS		DVDD_CORE
M				DVSS	DVSS	CSI0A_L2P_T1B	DVSS	DVSS	AVDD12_CSI1	DVSS	DVSS		DVSS
N	DVSS	CSI0A_L0P_T0A	CSI0A_L0N_T0B	CSI0A_L1P_T0C	CSI0A_L1N_T1A	CSI0A_L2N_T1C	DVSS			DVSS			DVSS

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Table 4-2 shows pin mapping on the top center part of the package.

Table 4-2 Ball map-top center

	14	15	16	17	18	19	20	21	22	23	24	25
A			EMI2_CS1		EMI2_CKE0		EMI3_CKE0		EMI3_CS1			EMI3_DMI0
B	EMI2_DQ6	DVSS	EMI2_CA0		EMI2_CKE1		EMI3_CKE1		EMI3_CA0	DVSS	EMI3_DQ6	DVSS
C	DVSS	DVSS	EMI2_CA1	DVSS	EMI2_CS0	DVSS	EMI3_CS0	DVSS	EMI3_CA1	DVSS	DVSS	DVSS
D	DVSS	DVSS	DVSS	EMI2_CA5	DVSS	NC	DVSS	DVSS	EMI3_CA3	DVSS	DVSS	EMI3_DQ5
E	DVSS	DVSS	DVSS	EMI2_CA4	DVSS	DVSS	DVSS	DVSS	EMI3_CA4	DVSS	DVSS	EMI3_DQ3
F	DVSS	EMI2_CA2	EMI2_CA3	DVSS	EMI2_CK_T	DVSS	EMI3_CK_T	DVSS	DVSS	NC	DVSS	DVSS
G	EMI2_DQ4	DVSS	NC	DVSS	EMI2_CK_C	DVSS	EMI3_CK_C	DVSS	EMI3_CA5	EMI3_CA2	DVSS	EMI3_DQ4
H	DVSS	DVSS	DVSS	DVSS	DVSS	NC	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS
J	DVSS	AVDDQ_EMI2	DVSS	AVDDQ_EMI2	DVSS	AVDDQ_EMI2	DVSS	AVDDQ_EMI2	DVSS	AVDDQ_EMI2	AVDD18_EMI2	DVSS
K	AVDDQ_EMI2	AVDD2_EMI2	AVDDQ_EMI2	AVDD2_EMI2	AVDDQ_EMI2	AVDD2_EMI2	AVDDQ_EMI2	AVDD2_EMI2	AVDDQ_EMI2	AVDD2_EMI2	AVDD075_EMI2	DVSS
L								DVDD_PROC_B		DVSS	AVDD18_PROC	DVSS
M	DVDD_MM	DVSS	DVDD_SRAM_MM	DVSS	DVDD_MM	DVDD_MM	DVDD_CORE	DVDD_PROC_B	DVDD_SRAM_PROC_B	DVSS	DVSS	DVDD_PROC_B
N	DVDD_MM	DVDD_MM	DVSS	DVDD_MM	DVSS	DVDD_MM	DVDD_CORE	DVDD_PROC_B	DVDD_PROC_B	DVSS	DVDD_PROC_B	DVDD_PROC_B

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Table 4-3 shows pin mapping on the top right part of the package.

Table 4-3 Ball map-top right

26	27	28	29	30	31	32	33	34	35	36	37	
	EMI3_DQ0		EMI3_DQ15		EMI3_DMI1	DVSS	EMI3_DQS1_T	EMI3_DQ9	DVSS	DUMMY	DUMMY	A
EMI3_DQ1	DVSS	EMI3_DQ7	DVSS	EMI3_DQ14	DVSS	DVSS	EMI3_DQS1_C	DVSS	DVSS	EMI2_RESET_N	DUMMY	B
DVSS	EMI3_DQ2	DVSS	EMI3_DQ11	DVSS	DVSS	EMI3_DQ13	DVSS	EMI3_DQ8	DVSS	DVSS	DVDD18_IOEMMC	C
DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	EMMC_DAT0	DVSS	EMMC_DAT4	EMMC_DAT2	EMMC_DAT7	D
DVSS	EMI3_DQS0_T	DVSS	EMI3_DQ12	EMI3_DQ10	DVSS	EMMC_DAT3	DVSS	EMMC_RSTB	EMMC_DSL	EMMC_DAT6		E
DVSS	EMI3_DQS0_C	DVSS	DVSS	DVSS	DVSS	EMMC_CLK	EMMC_CMD	DVSS	DVSS	EMMC_DAT1	EMMC_DAT5	F
DVSS	DVSS	DVSS	DVSS	I2SO2_D2	I2SO2_D1	I2SIN_D2	I2SIN_D1	DVSS	DVSS	I2SIN_MCK	DVDD18_IOLT	G
DVSS	DVDD18_VQPS	DVSS	DVSS	DVSS	KPCOL0	I2SO2_D3	I2SO2_BCK	I2SO2_MCK	I2SIN_D3	I2SIN_BCK		H
DVSS	DVSS	DVSS	DVSS	KPROW0	KPCOL1		I2SO2_D0	I2SO2_WS		I2SIN_WS	I2SIN_D0	J
DVDD_PROC_B	DVDD_PROC_B	DVDD_PROC_B	DVSS	KPROW1	PWRAP_SPI_CK	PWRAP_SPI_CSN	SPMI_M_SCL	PMIC_WATCHDOG	SPMI_M_SDA	SCL4	SDA4	K
DVDD_PROC_B	DVDD_PROC_B	DVDD_PROC_B	DVSS	PWRAP_SPI_MO	PWRAP_SPI_MI		PMIC_SRCLKENA0	PMIC_SRCLKENA1		SDA1		L
DVDD_PROC_B	DVDD_PROC_B	DVDD_PROC_B	DVSS	AUD_DAT_MISO0	SCP_VREQ_VAO	AUD_DAT_MISO1	AUD_CLK_MOSI	AUD_DAT_MOSI0	AUD_SYNC_MOSI	SCL1	DVSS	M
DVDD_SRAM_PROC_B	DVSS	DVSS	DVSS	DMIC1_CLK	DMIC1_DAT		AUD_DAT_MOSI1	DMIC2_CLK		DVSS	PMIC_RTC32K_CK	N

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Table 4-4 shows pin mapping on the middle left part of the package.

Table 4-4 Ball map-middle left

	1	2	3	4	5	6	7	8	9	10	11	12	13
P	CSI0B_L0N_T0B	CSI0B_L0P_T0A	CSI0B_L1P_T0C	CSI0B_L1N_T1A	CSI0B_L2P_T1B	CSI0B_L2N_T1C	DVSS	AVDD12_CSI0	DVSS	DVSS	DVSS		DVSS
R			DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS		DVDD_SRAM_MM
T	JTDO	JTRST	DVSS	JTDI	JTCK	JTMS	SPIM1_MISO	SPIM1_MOSI	SPIM1_CSB	SPIM1_CLK	SPIM0_CLK		DVSS
U		UART0_TXD	UART0_RXD	UART2_TXD	UART2_RXD		SPIM0_MIO2	SPIM0_MIO3	DVDD28_IODPI	GPIO01		DVDD_CORE	DVDD_CORE
V	UART1_TXD	UART1_RXD		GPIO09	GPIO10	SPIM0_CSB	SPIM0_MOSI	SPIM0_MISO				DVSS	AVDD18_PLLGP34
W	SDA3	SCL3	GPIO06	GPIO07	GPIO08	SDA0	GPIO05	GPIO11				DVSS	AVDD18_PLLGP34
Y		SCL2		SCL0	DSI1_DSI_TE	GPIO02	GPIO03	GPIO04	DSI0_LCM_RST	GPIO00	DISP_PWM1		DVDD_APU
AA	PCIE_CLKREQ_N	SDA2	PCIE_PERESET_N	PCIE_WAKE_N	DPI_D11	DPI_D12	DSI0_DSI_TE	DPI_D5	DISP_PWM0	DVDD18_IORM	DSI1_LCM_RST		DVDD_APU
AB	DPI_CK	DPI_DE	DPI_D4	DPI_D15	DPI_D9	DPI_D8	DPI_D7	DPI_D2	DPI_D0			DVSS	DVDD_SRAM_APU
AC				DPI_D3	DPI_D10	DPI_D13	DPI_D14	DPI_D6	DPI_D1			DVSS	DVDD_SRAM_GPU
AD	DVDD18_IODPI	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DPI_VSYNC	DPI_HSYNC	DVSS	DVDD_GPU
AE	AVDD12_AUXADC	AUXIN3	AUXIN2	AUXIN4	AUXIN5	AUXIN0	REFP	DVSS	DVSS	AVDD18_DSI	AVDD075_DRV_DSI	DVSS	DVDD_GPU

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Table 4-5 shows pin mapping on the middle center part of the package.

Table 4-5 Ball map-middle center

	14	15	16	17	18	19	20	21	22	23	24	25
P	DVDD_MM	DVDD_CORE	DVSS	DVDD_MM	DVSS	DVDD_MM	DVDD_MM	DVSS	DVSS	DVSS	DVDD_PROC_L	DVSS
R	DVDD_MM	DVDD_CORE	DVSS	DVDD_MM	DVSS	DVDD_MM	DVDD_MM	DVDD_SRAM_PROC_L	DVDD_PROC_L	DVSS	DVSS	DVDD_PROC_L
T	DVDD_MM	DVDD_MM	DVDD_MM	DVDD_MM	DVSS	DVDD_CORE			DVDD_PROC_L	DVSS	DVSS	DVDD_PROC_L
U	DVDD_CORE	DVDD_CORE	DVDD_CORE	DVDD_CORE	TN_APPLLGP	AVDD12_PLLGP1	DVDD_CORE	DVSS	DVDD_PROC_L	DVSS	DVDD_PROC_L	DVDD_PROC_L
V	AVDD12_PLLGP34	DVSS	DVDD_APU	DVDD_CORE	DVDD_CORE	TP_APPLLGP	AVDD18_PLLGP1	DVSS	DVDD_PROC_L	DVSS	DVDD_SRAM_PROC_L	DVSS
W	AVDD12_PLLGP34	DVSS	DVDD_APU	AVDD18_APU	DVSS	DVDD_CORE	DVDD_CORE	DVSS	DVSS	DVSS	DVDD_PROC_L	DVSS
Y	DVDD_APU	DVSS	DVDD_APU	DVDD_APU	DVSS	DVDD_CORE	DVDD_CORE	DVSS	DVDD_SRAM_CORE	DVDD_CORE	DVDD_CORE	DVDD_CORE
AA	DVDD_APU	DVSS	DVDD_APU	DVDD_APU	DVSS	DVDD_CORE	DVDD_CORE	DVSS	DVSS	DVDD_CORE	DVDD_CORE	DVSS
AB	DVDD_APU	DVSS	DVDD_APU	DVSS	DVSS	DVDD_CORE	DVDD_CORE	DVSS	DVSS	DVDD_CORE	DVDD_CORE	DVSS
AC	DVDD_GPU	DVDD_GPU	AVDD12_PLLGP2	AVDD18_PLLGP2	DVSS	DVDD_CORE	DVDD_CORE	DVSS	DVSS	DVDD_CORE	DVDD_CORE	DVSS
AD	DVDD_GPU	DVDD_GPU	DVDD_GPU	DVSS	DVSS	DVDD_ADSP	DVDD_ADSP	DVSS	DVDD_SRAM_CORE	DVDD_CORE	DVDD_CORE	DVSS
AE	DVDD_GPU	DVDD_GPU	DVDD_GPU	DVSS	DVSS	DVDD_ADSP	DVDD_ADSP	DVSS	DVSS	DVDD_CORE	DVDD_CORE	

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Table 4-6 shows pin mapping on the Middle Right part of the package.

Table 4-6 Ball map-middle right

26	27	28	29	30	31	32	33	34	35	36	37	
DVSS	DVSS	DVSS	DVSS	DMIC1_DAT_R	USB2_IDDIG	USB2_DRV_VBUS	DMIC2_DAT	USB0_VBUS_VALID	DMIC2_DAT_R	USB0_DRV_VBUS		P
DVDD_PROC_L	DVDD_PROC_L	DVSS	DVSS	USB2_VBUS_VALID	GPIO12		USB1_DRV_VBUS	USB1_IDDIG		USB0_IDDIG	DVDD18_IOLT	R
DVDD_PROC_L	DVDD_PROC_L	DVDD_PROC_L	DVSS	GPIO13	GPIO14	SYSRSTB	USB1_VBUS_VALID	TESTMODE	DVSS	DVSS	DVSS	T
DVDD_PROC_L	DVDD_PROC_L	AVDD18_USB_P2	AVDD33_USB_P2	DVSS	DVSS	GPIO15	AVDD33_USB_P0	DVSS	DVSS	USB_DM_P1	USB_DP_P1	U
DVSS	DVDD_PROC_L		DVSS	DVSS	DVSS	AVDD33_USB_P1	DVSS	USB_DP_P2	USB_DM_P2	DVSS		V
		AVDD18_USB_P0	AVDD12_USB_P0	DVSS	USB_DM_P0	USB_DP_P0	DVSS	DVSS	DVSS	SSUSB_RXN	SSUSB_RXP	W
	DVSS	AVDD12_USB_P1	AVDD12_USB_P2	DVSS	DVSS	DVSS	SSUSB_TXP	SSUSB_TXN	DVSS	DVSS		Y
DVSS	DVSS		AVDD18_USB_P1			DVSS	DVSS	DVSS	GPIO17	DVDD28_MSDC2		AA
	DVSS		DVSS	DVSS	PCM_DI	GPIO16	DPTX_HPD	HDMITX_PWR5V	MSDC2_DAT3	DVDD18_MSDC2	MSDC2_DAT2	AB
	DVSS	AVDD12_SSUSB	AVDD18_SSUSB	PCM_DO	PCM_SYNC	HDMITX_HTPLG	HDMITX_CEC		MSDC2_CMD			AC
DVSS		AVDD12_CKSQ	AVDD18_CKSQ	PCM_CLK	DVDD18_IOLM	HDMITX_SCL	HDMITX_SDA	DVSS	MSDC2_CLK	MSDC2_DAT1	MSDC2_DAT0	AD
	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	X26M_IN	DVSS	DVSS		AE

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Table 4-7 shows pin mapping on the Bottom Left part of the package.

Table 4-7 Ball map-bottom left

	1	2	3	4	5	6	7	8	9	10	11	12	13
AF	AVDD18_AUXADC	AUXIN1	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS		DVSS	DVDD_SRAM_GPU
AG				DVSS	DSI0_D0P_T0C	DSI0_D2N_T0B	DSI0_D2P_T0A	DVSS	DVSS		DVSS		
AH	DVSS	DSI0_D3N	DSI0_D1N_T2B	DSI0_D1P_T2A	DSI0_D0N_T1A	DSI0_CKP_T1B	DSI0_CKN_T1C	DVSS	DVSS	AVDD12_DSI	AVDD18_PCIE	DVSS	
AJ			DSI0_D3P_T2C	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS		AVDD12_PCIE	DVSS	DVSS
AK					DSI1_D0N_T1A	DSI1_CKN_T1C	DSI1_CKP_T1B	DSI1_D3N	DVSS	DVSS	DVSS	DVSS	DVSS
AL	DVSS	DVSS	DSI1_D2P_T0A	DSI1_D2N_T0B	DSI1_D0P_T0C	DSI1_D1N_T2B	DSI1_D1P_T2A	DSI1_D3P_T2C	DVSS	DVSS	DVSS	DVSS	EMI1_DQ4
AM	PCIE_LN0_TXP	PCIE_LN0_TXN	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	EMI1_DQS0_C	DVSS	DVSS
AN		DVSS	PCIE_CKN	PCIE_CKP	DVSS	DVSS	DVSS	EMI1_DQ10	EMI1_DQ12	DVSS	EMI1_DQS0_T	DVSS	EMI1_DQ3
AP	PCIE_LN0_RXN	PCIE_LN0_RXP	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	EMI1_DQ5
AR		DVSS	EMI0_TP	EMI1_DQ8	DVSS	EMI1_DQ13	DVSS	DVSS	EMI1_DQ11	DVSS	EMI1_DQ2	DVSS	DVSS
AT	DUMMY	EMI0_EXTR	DVSS	DVSS	EMI1_DQS1_C	DVSS	DVSS	EMI1_DQ14	DVSS	EMI1_DQ7	DVSS	EMI1_DQ1	DVSS
AU	DUMMY	DUMMY	DVSS	EMI1_DQ9	EMI1_DQS1_T	DVSS	EMI1_DMI1		EMI1_DQ15		EMI1_DQ0		EMI1_DMI0

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Table 4-8 shows pin mapping on the Bottom Center part of the package.

Table 4-8 Ball map-bottom center

	14	15	16	17	18	19	20	21	22	23	24	25
AF	DVDD_GPU	DVDD_GPU	DVDD_GPU	DVDD_GPU	DVSS	DVDD_ADSP	DVDD_ADSP	DVSS	DVDD_SRAM_CORE	DVDD_CORE	DVDD_CORE	
AG	DVDD_CORE											
AH	AVDD075_EMI0	AVDD2_EMI0	AVDDQ_EMI0	AVDD2_EMI0	AVDDQ_EMI0	AVDD2_EMI0	AVDDQ_EMI0	AVDD2_EMI0	AVDDQ_EMI0	AVDD2_EMI0	AVDD075_EMI0	AVDD18_EMI0
AJ	AVDD12_EMI0	AVDDQ_EMI0	DVSS	AVDDQ_EMI0	DVSS	AVDDQ_EMI0	DVSS	AVDDQ_EMI0	DVSS	AVDDQ_EMI0	AVDDQ_EMI0	DVSS
AK	DVSS	DVSS	DVSS	DVSS	DVSS	NC	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS
AL	DVSS	EMI1_CA2	EMI1_CA5	DVSS	EMI1_CK_C	DVSS	EMI0_CK_C	DVSS	NC	DVSS	EMI0_DQ4	EMI0_DQ2
AM	DVSS	NC	DVSS	DVSS	EMI1_CK_T	DVSS	EMI0_CK_T	DVSS	EMI0_CA3	EMI0_CA2	DVSS	DVSS
AN	DVSS	DVSS	EMI1_CA4	DVSS	DVSS	DVSS	DVSS	EMI0_CA4	DVSS	DVSS	DVSS	EMI0_DQ5
AP	DVSS	DVSS	EMI1_CA3	DVSS	DVSS	NC	DVSS	EMI0_CA5	DVSS	DVSS	DVSS	EMI0_DQ3
AR	DVSS	DVSS	EMI1_CA1	DVSS	EMI1_CS0	DVSS	EMI0_CS0	DVSS	EMI0_CA1	DVSS	DVSS	DVSS
AT	EMI1_DQ6	DVSS	EMI1_CA0		EMI1_CKE1		EMI0_CKE1		EMI0_CA0	DVSS	EMI0_DQ6	DVSS
AU			EMI1_CS1		EMI1_CKE0		EMI0_CKE0		EMI0_CS1			EMI0_DMI0

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Table 4-9 shows pin mapping on the Bottom Right part of the package.

Table 4-9 Ball map-bottom right

DVSS	DVSS	DVSS	DVSS	DVSS	EDP_LN1_TXN	EDP_LN1_TXP	DVSS	DVSS	DVSS	EDPAUXP	EDPAUXN	AF
AVDD18_EDPTX	AVDD12_EDPTX	DVSS	EDP_LN0_TXN	EDP_LN0_TXP	DVSS	DVSS	DVSS	DVSS	DP_LN0_TXP			AG
		AVDD18_DPTX	DVSS	DVSS	DP_LN1_TXN	DP_LN1_TXP	DVSS	DVSS	DP_LN0_TXN			AH
DVSS	DVSS	DVSS	AVDD12_DPTX	DVSS	DVSS	DVSS	DP_LN2_TXN	DP_LN2_TXP	DVSS	DPAUXP	DPAUXN	AJ
DVSS	DVSS	DVSS	DVSS	DVSS	DP_LN3_TXN	DP_LN3_TXP	DVSS	DVSS	HDMITX21_CH2_P			AK
DVSS	DVSS	AVDD12_ HDMITX21	AVDD18_ HDMITX21		DVSS	DVSS	DVSS	DVSS	HDMITX21_CH2_ M			AL
DVSS	EMI0_DQS0_T	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	HDMITX21_CH1_ P	HDMITX21_CH1_ M	AM
DVSS	EMI0_DQS0_C	DVSS	EMI0_DQ11	DVSS	EMI0_DQ9	DVSS	DVSS	HDMITX21_CH0_ M	HDMITX21_CH0_P			AN
DVSS	DVSS	DVSS	DVSS	EMI0_DQ10	EMI0_DQ13	DVSS	DVSS	DVSS		DVSS	DVSS	AP
DVSS	DVSS	DVSS	EMI0_DQ12	DVSS	DVSS	EMI0_DQS1_C	DVSS	HDMITX21_CLK_ P	HDMITX21_CLK_ M			AR
EMI0_DQ1	DVSS	EMI0_DQ7	DVSS	EMI0_DQ14	DVSS	EMI0_DQS1_T	DVSS	DVSS	DVSS	DVSS	DUMMY	AT
	EMI0_DQ0		EMI0_DQ15		EMI0_DMI1	DVSS	DVSS	EMI0_DQ8	EMI0_RESET_N	DUMMY	DUMMY	AU
26	27	28	29	30	31	32	33	34	35	36	37	

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4.1.2 DDR4

Table 4-10 shows pin mapping on the top left part of the package.

Table 4-10 Ball map-top left

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	DUMMY	DUMMY	EMI2_TP	EMI2_DQ9	DVSS	DVSS	EMI2_DMI0		EMI2_DQ15		EMI2_DQ10		EMI2_DMI1
B	DUMMY	EMI2_EXTR	DVSS	DVSS	DVSS	EMI2_DQS1_T	DVSS	EMI2_DQ11	DVSS	EMI2_DQ1	DVSS	EMI2_DQ8	DVSS
C		DVSS	MSDC1_DAT3	MSDC1_DAT2	DVSS	EMI2_DQS1_C	DVSS	DVSS	EMI2_DQ7	DVSS	DVSS	DVSS	DVSS
D	MSDC1_DAT1	MSDC1_DAT0	MSDC1_CMD	MSDC1_CLK	DVSS	DVSS	EMI2_DQ5	EMI2_DQ3	DVSS	DVSS	DVSS	DVSS	EMI2_DQ2
E	DVDD18_MSDC1	SPIM2_MISO	CMMPDN1	CMMCLK0	CMMCLK1	DVSS	EMI2_DQ13	DVSS	EMI2_DQ6	DVSS	EMI2_DQS0_C	DVSS	EMI2_DQ0
F		SPIM2_MOSI		CMMCLK2	SCL5	SDA5	DVSS	DVSS	DVSS	DVSS	EMI2_DQS0_T	DVSS	DVSS
G	SPIM2_CLK	SPIM2_CSB	CMMRST0	CMMPDN0	CMMRST1	SDA6	DVDD28_MSDC1	DVSS	DVSS	DVSS	DVSS	DVSS	EMI2_DQ14
H				DVSS	DVSS	DVSS	SCL6	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS
J	DVSS	CSI1A_L1P_T0C	CSI1A_L1N_T1A	CSI1A_L0N_T0B	CSI1A_L0P_T0A	DVSS	DVSS	DVSS	DVSS	DVSS	DVDD18_IORT	DVSS	AVDD12_EMI2
K			CSI1B_L0N_T0B	DVSS	CSI1B_L0P_T0A	CSI1A_L2N_T1C	CSI1A_L2P_T1B	DVSS	DVSS	DVSS	DVSS		AVDD075_EMI2
L			CSI1B_L1P_T0C	CSI1B_L1N_T1A	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS		DVDD_CORE
M				DVSS	DVSS	CSI0A_L2P_T1B	DVSS	DVSS	AVDD12_CSI1	DVSS	DVSS		DVSS
N	DVSS	CSI0A_L0P_T0A	CSI0A_L0N_T0B	CSI0A_L1P_T0C	CSI0A_L1N_T1A	CSI0A_L2N_T1C	DVSS			DVSS			DVSS

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Table 4-11 shows pin mapping on the top center part of the package.

Table 4-11 Ball map-top center

	14	15	16	17	18	19	20	21	22	23	24	25
A			EMI2_CA3		EMI2_CKE0		EMI3_CKE0		EMI2_CA4			EMI3_DMI0
B	EMI2_DQ12	DVSS	EMI2_CA12		EMI2_WE_N		EMI2_ACT_N		EMI2_BG0	DVSS	EMI3_DQ13	DVSS
C	DVSS	DVSS	EMI2_RAS_N	DVSS	EMI2_CS0	DVSS	EMI3_CS0	DVSS	EMI2_CA10	DVSS	DVSS	DVSS
D	DVSS	DVSS	DVSS	EMI2_CA1	DVSS	EMI2_ODT	DVSS	DVSS	EMI2_CA6	DVSS	DVSS	EMI3_DQ5
E	DVSS	DVSS	DVSS	EMI2_BA1	DVSS	DVSS	DVSS	DVSS	EMI2_CA0	DVSS	DVSS	EMI3_DQ3
F	DVSS	EMI2_CA7	EMI2_CA5	DVSS	EMI2_CK_T	DVSS	EMI2_CA13	DVSS	DVSS	EMI2_CAS_N	DVSS	DVSS
G	EMI2_DQ4	DVSS	EMI2_CA9	DVSS	EMI2_CK_C	DVSS	EMI2_CA2	DVSS	EMI2_BA0	EMI2_CA8	DVSS	EMI3_DQ1
H	DVSS	DVSS	DVSS	DVSS	DVSS	EMI2_CA11	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS
J	DVSS	AVDDQ_EMI2	DVSS	AVDDQ_EMI2	DVSS	AVDDQ_EMI2	DVSS	AVDDQ_EMI2	DVSS	AVDDQ_EMI2	AVDD18_EMI2	DVSS
K	AVDDQ_EMI2	AVDD2_EMI2	AVDDQ_EMI2	AVDD2_EMI2	AVDDQ_EMI2	AVDD2_EMI2	AVDDQ_EMI2	AVDD2_EMI2	AVDDQ_EMI2	AVDD2_EMI2	AVDD075_EMI2	DVSS
L								DVDD_PROC_B		DVSS	AVDD18_PROC	DVSS
M	DVDD_MM	DVSS	DVDD_SRAM_MM	DVSS	DVDD_MM	DVDD_MM	DVDD_CORE	DVDD_PROC_B	DVDD_SRAM_PROC_B	DVSS	DVSS	DVDD_PROC_B
N	DVDD_MM	DVDD_MM	DVSS	DVDD_MM	DVSS	DVDD_MM	DVDD_CORE	DVDD_PROC_B	DVDD_PROC_B	DVSS	DVDD_PROC_B	DVDD_PROC_B

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Table 4-12 shows pin mapping on the top right part of the package.

Table 4-12 Ball map-top right

26	27	28	29	30	31	32	33	34	35	36	37	
	EMI3_DQ15		EMI3_DQ8		EMI3_DMI1	DVSS	EMI3_DQS0_T	EMI3_DQ0	DVSS	DUMMY	DUMMY	A
EMI3_DQ11	DVSS	EMI3_DQ10	DVSS	EMI3_DQ12	DVSS	DVSS	EMI3_DQS0_C	DVSS	DVSS	EMI2_RESET_N	DUMMY	B
DVSS	EMI3_DQ9	DVSS	EMI3_DQ7	DVSS	DVSS	EMI3_DQ4	DVSS	EMI3_DQ14	DVSS	DVSS	DVDD18_IOEMMC	C
DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	EMMC_DAT0	DVSS	EMMC_DAT4	EMMC_DAT2	EMMC_DAT7	D
DVSS	EMI3_DQS1_T	DVSS	EMI3_DQ6	EMI3_DQ2	DVSS	EMMC_DAT3	DVSS	EMMC_RSTB	EMMC_DSL	EMMC_DAT6		E
DVSS	EMI3_DQS1_C	DVSS	DVSS	DVSS	DVSS	EMMC_CLK	EMMC_CMD	DVSS	DVSS	EMMC_DAT1	EMMC_DAT5	F
DVSS	DVSS	DVSS	DVSS	I2SO2_D2	I2SO2_D1	I2SIN_D2	I2SIN_D1	DVSS	DVSS	I2SIN_MCK	DVDD18_IOLT	G
DVSS	DVDD18_VQPS	DVSS	DVSS	DVSS	KPCOL0	I2SO2_D3	I2SO2_BCK	I2SO2_MCK	I2SIN_D3	I2SIN_BCK		H
DVSS	DVSS	DVSS	DVSS	KPROW0	KPCOL1		I2SO2_D0	I2SO2_WS		I2SIN_WS	I2SIN_D0	J
DVDD_PROC_B	DVDD_PROC_B	DVDD_PROC_B	DVSS	KPROW1	PWRAP_SPI_CK	PWRAP_SPI_CSN	SPMI_M_SCL	PMIC_WATCHDOG	SPMI_M_SDA	SCL4	SDA4	K
DVDD_PROC_B	DVDD_PROC_B	DVDD_PROC_B	DVSS	PWRAP_SPI_MO	PWRAP_SPI_MI		PMIC_SRCLKENA0	PMIC_SRCLKENA1		SDA1		L
DVDD_PROC_B	DVDD_PROC_B	DVDD_PROC_B	DVSS	AUD_DAT_MISO0	SCP_VREQ_VAO	AUD_DAT_MISO1	AUD_CLK_MOSI	AUD_DAT_MOSI0	AUD_SYNC_MOSI	SCL1	DVSS	M
DVDD_SRAM_PROC_B	DVSS	DVSS	DVSS	DMIC1_CLK	DMIC1_DAT		AUD_DAT_MOSI1	DMIC2_CLK		DVSS	PMIC_RTC32K_CK	N

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Table 4-13 shows pin mapping on the middle left part of the package.

Table 4-13 Ball map-middle left

	1	2	3	4	5	6	7	8	9	10	11	12	13
P	CSI0B_L0N_T0B	CSI0B_L0P_T0A	CSI0B_L1P_T0C	CSI0B_L1N_T1A	CSI0B_L2P_T1B	CSI0B_L2N_T1C	DVSS	AVDD12_CSI0	DVSS	DVSS	DVSS		DVSS
R			DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS		DVDD_SRAM_MM
T	JTDO	JTRST	DVSS	JTDI	JTCK	JTMS	SPIM1_MISO	SPIM1_MOSI	SPIM1_CSB	SPIM1_CLK	SPIM0_CLK		DVSS
U		UART0_TXD	UART0_RXD	UART2_TXD	UART2_RXD		SPIM0_MIO2	SPIM0_MIO3	DVDD28_IODPI	GPIO01		DVDD_CORE	DVDD_CORE
V	UART1_TXD	UART1_RXD		GPIO09	GPIO10	SPIM0_CSB	SPIM0_MOSI	SPIM0_MISO				DVSS	AVDD18_PLLGP34
W	SDA3	SCL3	GPIO06	GPIO07	GPIO08	SDA0	GPIO05	GPIO11				DVSS	AVDD18_PLLGP34
Y		SCL2		SCL0	DSI1_DSI_TE	GPIO02	GPIO03	GPIO04	DSI0_LCM_RST	GPIO00	DISP_PWM1		DVDD_APU
AA	PCIE_CLKREQ_N	SDA2	PCIE_PERESET_N	PCIE_WAKE_N	DPI_D11	DPI_D12	DSI0_DSI_TE	DPI_D5	DISP_PWM0	DVDD18_IORM	DSI1_LCM_RST		DVDD_APU
AB	DPI_CK	DPI_DE	DPI_D4	DPI_D15	DPI_D9	DPI_D8	DPI_D7	DPI_D2	DPI_D0			DVSS	DVDD_SRAM_APU
AC				DPI_D3	DPI_D10	DPI_D13	DPI_D14	DPI_D6	DPI_D1			DVSS	DVDD_SRAM_GPU
AD	DVDD18_IODPI	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DPI_VSYNC	DPI_HSYNC	DVSS	DVDD_GPU
AE	AVDD12_AUXADC	AUXIN3	AUXIN2	AUXIN4	AUXIN5	AUXIN0	REFP	DVSS	DVSS	AVDD18_DSI	AVDD075_DRV_DSI	DVSS	DVDD_GPU

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Table 4-14 shows pin mapping on the middle center part of the package.

Table 4-14 Ball map-middle center

	14	15	16	17	18	19	20	21	22	23	24	25
P	DVDD_MM	DVDD_CORE	DVSS	DVDD_MM	DVSS	DVDD_MM	DVDD_MM	DVSS	DVSS	DVSS	DVDD_PROC_L	DVSS
R	DVDD_MM	DVDD_CORE	DVSS	DVDD_MM	DVSS	DVDD_MM	DVDD_MM	DVDD_SRAM_PROC_L	DVDD_PROC_L	DVSS	DVSS	DVDD_PROC_L
T	DVDD_MM	DVDD_MM	DVDD_MM	DVDD_MM	DVSS	DVDD_CORE			DVDD_PROC_L	DVSS	DVSS	DVDD_PROC_L
U	DVDD_CORE	DVDD_CORE	DVDD_CORE	DVDD_CORE	TN_APPLLGP	AVDD12_PLLGP1	DVDD_CORE	DVSS	DVDD_PROC_L	DVSS	DVDD_PROC_L	DVDD_PROC_L
V	AVDD12_PLLGP34	DVSS	DVDD_APU	DVDD_CORE	DVDD_CORE	TP_APPLLGP	AVDD18_PLLGP1	DVSS	DVDD_PROC_L	DVSS	DVDD_SRAM_PROC_L	DVSS
W	AVDD12_PLLGP34	DVSS	DVDD_APU	AVDD18_APU	DVSS	DVDD_CORE	DVDD_CORE	DVSS	DVSS	DVSS	DVDD_PROC_L	DVSS
Y	DVDD_APU	DVSS	DVDD_APU	DVDD_APU	DVSS	DVDD_CORE	DVDD_CORE	DVSS	DVDD_SRAM_CORE	DVDD_CORE	DVDD_CORE	DVDD_CORE
AA	DVDD_APU	DVSS	DVDD_APU	DVDD_APU	DVSS	DVDD_CORE	DVDD_CORE	DVSS	DVSS	DVDD_CORE	DVDD_CORE	DVSS
AB	DVDD_APU	DVSS	DVDD_APU	DVSS	DVSS	DVDD_CORE	DVDD_CORE	DVSS	DVSS	DVDD_CORE	DVDD_CORE	DVSS
AC	DVDD_GPU	DVDD_GPU	AVDD12_PLLGP2	AVDD18_PLLGP2	DVSS	DVDD_CORE	DVDD_CORE	DVSS	DVSS	DVDD_CORE	DVDD_CORE	DVSS
AD	DVDD_GPU	DVDD_GPU	DVDD_GPU	DVSS	DVSS	DVDD_ADSP	DVDD_ADSP	DVSS	DVDD_SRAM_CORE	DVDD_CORE	DVDD_CORE	DVSS
AE	DVDD_GPU	DVDD_GPU	DVDD_GPU	DVSS	DVSS	DVDD_ADSP	DVDD_ADSP	DVSS	DVSS	DVDD_CORE	DVDD_CORE	

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Table 4-15 shows pin mapping on the middle right part of the package.

Table 4-15 Ball map-middle right

26	27	28	29	30	31	32	33	34	35	36	37	
DVSS	DVSS	DVSS	DVSS	DMIC1_DAT_R	USB2_IDDIG	USB2_DRV_VBUS	DMIC2_DAT	USB0_VBUS_VALID	DMIC2_DAT_R	USB0_DRV_VBUS		P
DVDD_PROC_L	DVDD_PROC_L	DVSS	DVSS	USB2_VBUS_VALID	GPIO12		USB1_DRV_VBUS	USB1_IDDIG		USB0_IDDIG	DVDD18_IOLT	R
DVDD_PROC_L	DVDD_PROC_L	DVDD_PROC_L	DVSS	GPIO13	GPIO14	SYSRSTB	USB1_VBUS_VALID	TESTMODE	DVSS	DVSS	DVSS	T
DVDD_PROC_L	DVDD_PROC_L	AVDD18_USB_P2	AVDD33_USB_P2	DVSS	DVSS	GPIO15	AVDD33_USB_P0	DVSS	DVSS	USB_DM_P1	USB_DP_P1	U
DVSS	DVDD_PROC_L		DVSS	DVSS	DVSS	AVDD33_USB_P1	DVSS	USB_DP_P2	USB_DM_P2	DVSS		V
		AVDD18_USB_P0	AVDD12_USB_P0	DVSS	USB_DM_P0	USB_DP_P0	DVSS	DVSS	DVSS	SSUSB_RXN	SSUSB_RXP	W
	DVSS	AVDD12_USB_P1	AVDD12_USB_P2	DVSS	DVSS	DVSS	SSUSB_TXP	SSUSB_TXN	DVSS	DVSS		Y
DVSS	DVSS		AVDD18_USB_P1			DVSS	DVSS	DVSS	GPIO17	DVDD28_MSDC2		AA
	DVSS		DVSS	DVSS	PCM_DI	GPIO16	DPTX_HPD	HDMITX_PWR5V	MSDC2_DAT3	DVDD18_MSDC2	MSDC2_DAT2	AB
	DVSS	AVDD12_SSUSB	AVDD18_SSUSB	PCM_DO	PCM_SYNC	HDMITX_HTPLG	HDMITX_CEC		MSDC2_CMD			AC
DVSS		AVDD12_CKSQ	AVDD18_CKSQ	PCM_CLK	DVDD18_IOLM	HDMITX_SCL	HDMITX_SDA	DVSS	MSDC2_CLK	MSDC2_DAT1	MSDC2_DAT0	AD
	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	X26M_IN	DVSS	DVSS		AE

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Table 4-16 shows pin mapping on the bottom left part of the package.

Table 4-16 Ball map-bottom left

	1	2	3	4	5	6	7	8	9	10	11	12	13
AF	AVDD18_AUXADC	AUXIN1	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS		DVSS	DVDD_SRAM_GPU
AG				DVSS	DSI0_D0P_T0C	DSI0_D2N_T0B	DSI0_D2P_T0A	DVSS	DVSS		DVSS		
AH	DVSS	DSI0_D3N	DSI0_D1N_T2B	DSI0_D1P_T2A	DSI0_D0N_T1A	DSI0_CKP_T1B	DSI0_CKN_T1C	DVSS	DVSS	AVDD12_DSI	AVDD18_PCIE	DVSS	
AJ			DSI0_D3P_T2C	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS		AVDD12_PCIE	DVSS	DVSS
AK					DSI1_D0N_T1A	DSI1_CKN_T1C	DSI1_CKP_T1B	DSI1_D3N	DVSS	DVSS	DVSS	DVSS	DVSS
AL	DVSS	DVSS	DSI1_D2P_T0A	DSI1_D2N_T0B	DSI1_D0P_T0C	DSI1_D1N_T2B	DSI1_D1P_T2A	DSI1_D3P_T2C	DVSS	DVSS	DVSS	DVSS	EMI1_DQ1
AM	PCIE_LN0_TXP	PCIE_LN0_TXN	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	EMI1_DQS1_C	DVSS	DVSS
AN		DVSS	PCIE_CKN	PCIE_CKP	DVSS	DVSS	DVSS	EMI1_DQ2	EMI1_DQ6	DVSS	EMI1_DQS1_T	DVSS	EMI1_DQ3
AP	PCIE_LN0_RXN	PCIE_LN0_RXP	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	EMI1_DQ5
AR		DVSS	EMI0_TP	EMI1_DQ14	DVSS	EMI1_DQ4	DVSS	DVSS	EMI1_DQ7	DVSS	EMI1_DQ9	DVSS	DVSS
AT	DUMMY	EMI0_EXTR	DVSS	DVSS	EMI1_DQS0_C	DVSS	DVSS	EMI1_DQ12	DVSS	EMI1_DQ10	DVSS	EMI1_DQ11	DVSS
AU	DUMMY	DUMMY	DVSS	EMI1_DQ0	EMI1_DQS0_T	DVSS	EMI1_DMI1		EMI1_DQ8		EMI1_DQ15		EMI1_DMI0

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Table 4-17 shows pin mapping on the Bottom Center part of the package.

Table 4-17 Ball map-bottom center

	14	15	16	17	18	19	20	21	22	23	24	25
AF	DVDD_GPU	DVDD_GPU	DVDD_GPU	DVDD_GPU	DVSS	DVDD_ADSP	DVDD_ADSP	DVSS	DVDD_SRAM_CORE	DVDD_CORE	DVDD_CORE	
AG	DVDD_CORE											
AH	AVDD075_EMI0	AVDD2_EMI0	AVDDQ_EMI0	AVDD2_EMI0	AVDDQ_EMI0	AVDD2_EMI0	AVDDQ_EMI0	AVDD2_EMI0	AVDDQ_EMI0	AVDD2_EMI0	AVDD075_EMI0	AVDD18_EMI0
AJ	AVDD12_EMI0	AVDDQ_EMI0	DVSS	AVDDQ_EMI0	DVSS	AVDDQ_EMI0	DVSS	AVDDQ_EMI0	DVSS	AVDDQ_EMI0	AVDDQ_EMI0	DVSS
AK	DVSS	DVSS	DVSS	DVSS	DVSS	EMI0_CA11	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS
AL	DVSS	EMI0_CA8	EMI0_BA0	DVSS	EMI0_CA2	DVSS	EMI0_CK_C	DVSS	EMI0_CA9	DVSS	EMI0_DQ4	EMI0_DQ14
AM	DVSS	EMI0_CAS_N	DVSS	DVSS	EMI0_CA13	DVSS	EMI0_CK_T	DVSS	EMI0_CA5	EMI0_CA7	DVSS	DVSS
AN	DVSS	DVSS	EMI0_CA0	DVSS	DVSS	DVSS	DVSS	EMI0_BA1	DVSS	DVSS	DVSS	EMI0_DQ0
AP	DVSS	DVSS	EMI0_CA6	DVSS	DVSS	EMI0_ODT	DVSS	EMI0_CA1	DVSS	DVSS	DVSS	EMI0_DQ2
AR	DVSS	DVSS	EMI0_CA10	DVSS	EMI1_CS0	DVSS	EMI0_CS0	DVSS	EMI0_RAS_N	DVSS	DVSS	DVSS
AT	EMI1_DQ13	DVSS	EMI0_BG0		EMI0_ACT_N		EMI0_WE_N		EMI0_CA12	DVSS	EMI0_DQ12	DVSS
AU			EMI0_CA4		EMI1_CKE0		EMI0_CKE0		EMI0_CA3			EMI0_DMI1

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Table 4-18 shows pin mapping on the Bottom Right part of the package.

Table 4-18 Ball map-bottom right

DVSS	DVSS	DVSS	DVSS	DVSS	EDP_LN1_TXN	EDP_LN1_TXP	DVSS	DVSS	DVSS	EDPAUXP	EDPAUXN	AF
AVDD18_EDPTX	AVDD12_EDPTX	DVSS	EDP_LN0_TXN	EDP_LN0_TXP	DVSS	DVSS	DVSS	DVSS	DP_LN0_TXP			AG
		AVDD18_DPTX	DVSS	DVSS	DP_LN1_TXN	DP_LN1_TXP	DVSS	DVSS	DP_LN0_TXN			AH
DVSS	DVSS	DVSS	AVDD12_DPTX	DVSS	DVSS	DVSS	DP_LN2_TXN	DP_LN2_TXP	DVSS	DPAUXP	DPAUXN	AJ
DVSS	DVSS	DVSS	DVSS	DVSS	DP_LN3_TXN	DP_LN3_TXP	DVSS	DVSS	HDMITX21_CH2_P			AK
DVSS	DVSS	AVDD12_ HDMITX21	AVDD18_ HDMITX21		DVSS	DVSS	DVSS	DVSS	HDMITX21_CH2_ M			AL
DVSS	EMI0_DQS0_T	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	HDMITX21_CH1_ P	HDMITX21_CH1_ M	AM
DVSS	EMI0_DQS0_C	DVSS	EMI0_DQ6	DVSS	EMI0_DQ13	DVSS	DVSS	HDMITX21_CH0_ M	HDMITX21_CH0_P			AN
DVSS	DVSS	DVSS	DVSS	EMI0_DQ3	EMI0_DQ5	DVSS	DVSS	DVSS		DVSS	DVSS	AP
DVSS	DVSS	DVSS	EMI0_DQ7	DVSS	DVSS	EMI0_DQS1_C	DVSS	HDMITX21_CLK_ P	HDMITX21_CLK_ M			AR
EMI0_DQ8	DVSS	EMI0_DQ1	DVSS	EMI0_DQ11	DVSS	EMI0_DQS1_T	DVSS	DVSS	DVSS	DVSS	DUMMY	AT
	EMI0_DQ10		EMI0_DQ15		EMI0_DMI0	DVSS	DVSS	EMI0_DQ9	EMI0_RESET_N	DUMMY	DUMMY	AU
26	27	28	29	30	31	32	33	34	35	36	37	

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4.2 Pin Characteristics

Table 4-19 describes the pin characteristics and the multiplexed signals on each ball.

Table 4-19 Pin characteristics

Ball name	Ball location	Signal name	Signal type	Aux. function	Reset function	Buffer type	Power domain	PU/PD reset	IO reset
GPIO00	Y10	GPIO0	DIO	0	0		DVDD18_IORM	OFF	I
		TP_GPIO0_AO	DIO	1					
		SPIM5_CSB	DO	2					
		UTXD1	DO	3					
		DMIC3_CLK	DO	4					
		I2SIN_MCK	DIO	5					
		I2SO2_MCK	DO	6					
GPIO01	U10	GPIO1	DIO	0	0		DVDD18_IORM	OFF	I
		TP_GPIO1_AO	DIO	1					
		SPIM5_CLK	DO	2					
		URXD1	DI	3					
		DMIC3_DAT	DI	4					
		I2SIN_BCK	DIO	5					
		I2SO2_BCK	DIO	6					

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Ball name	Ball location	Signal name	Signal type	Aux. function	Reset function	Buffer type	Power domain	PU/PD reset	IO reset
GPIO02	Y6	GPIO2	DIO	0	0		DVDD18_IORM	OFF	I
		TP_GPIO2_AO	DIO	1					
		SPIM5_MOSI	DIO	2					
		URTS1	DO	3					
		DMIC3_DAT_R	DI	4					
		I2SIN_WS	DIO	5					
		I2SO2_WS	DIO	6					
GPIO03	Y7	GPIO3	DIO	0	0		DVDD18_IORM	OFF	I
		TP_GPIO3_AO	DIO	1					
		SPIM5_MISO	DIO	2					
		UCTS1	DI	3					
		DMIC4_CLK	DO	4					
		I2SIN_D0	DI	5					
		I2SO2_D0	DO	6					
GPIO04	Y8	GPIO4	DIO	0	0		DVDD18_IORM	OFF	I
		TP_GPIO4_AO	DIO	1					
		SPDIF_IN2	DI	2					
		I2SO1_MCK	DO	3					
		DMIC4_DAT	DI	4					
		I2SIN_D1	DI	5					
		I2SO2_D1	DO	6					

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Ball name	Ball location	Signal name	Signal type	Aux. function	Reset function	Buffer type	Power domain	PU/PD reset	IO reset
GPIO05	W7	GPIO5	DIO	0	0		DVDD18_IORM	OFF	I
		TP_GPIO5_AO	DIO	1					
		SPDIF_IN1	DI	2					
		I2SO1_BCK	DO	3					
		DMIC4_DAT_R	DI	4					
		I2SIN_D2	DI	5					
		I2SO2_D2	DO	6					
GPIO06	W3	GPIO6	DIO	0	0		DVDD18_IORM	OFF	I
		TP_GPIO6_AO	DIO	1					
		SPDIF_IN0	DI	2					
		I2SO1_WS	DO	3					
		DMIC1_CLK	DO	4					
		I2SIN_D3	DI	5					
		I2SO2_D3	DO	6					
GPIO07	W4	GPIO7	DIO	0	0		DVDD18_IORM	OFF	I
		TP_GPIO7_AO	DIO	1					
		SPIM3_CSB	DO	2					
		TDMIN_MCK	DIO	3					
		DMIC1_DAT	DI	4					
		CMVREF0	DO	5					
		CLKM0	DO	6					

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Ball name	Ball location	Signal name	Signal type	Aux. function	Reset function	Buffer type	Power domain	PU/PD reset	IO reset
GPIO08	W5	GPIO8	DIO	0	0		DVDD18_IORM	OFF	I
		TP_GPIO0_AO	DIO	1					
		SPIM3_CLK	DO	2					
		TDMIN_BCK	DIO	3					
		DMIC1_DAT_R	DI	4					
		CMVREF1	DO	5					
		CLKM1	DO	6					
GPIO09	V4	GPIO9	DIO	0	0		DVDD18_IORM	OFF	I
		TP_GPIO1_AO	DIO	1					
		SPIM3_MOSI	DIO	2					
		TDMIN_LRCK	DIO	3					
		DMIC2_CLK	DO	4					
		CMFLASH0	DO	5					
		PWM_0	DO	6					
GPIO10	V5	GPIO10	DIO	0	0		DVDD18_IORM	OFF	I
		TP_GPIO2_AO	DIO	1					
		SPIM3_MISO	DIO	2					
		TDMIN_DI	DI	3					
		DMIC2_DAT	DI	4					
		CMFLASH1	DO	5					
		PWM_1	DO	6					

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Ball name	Ball location	Signal name	Signal type	Aux. function	Reset function	Buffer type	Power domain	PU/PD reset	IO reset
GPIO11	W8	GPIO11	DIO	0	0		DVDD18_IORM	OFF	I
		TP_GPIO3_AO	DIO	1					
		SPDIF_OUT	DO	2					
		I2SO1_D0	DO	3					
		DMIC2_DAT_R	DI	4					
		CMVREF6	DO	6					
GPIO12	R31	GPIO12	DIO	0	0		DVDD18_IOLT	OFF	I
		TP_GPIO4_AO	DIO	1					
		SPIM4_CSB	DO	2					
		HDMITX20_HTPLG	DI	7					
GPIO13	T30	GPIO13	DIO	0	0		DVDD18_IOLT	OFF	I
		TP_GPIO5_AO	DIO	1					
		SPIM4_CLK	DO	2					
		HDMITX20_CEC	DIO	7					
GPIO14	T31	GPIO14	DIO	0	0		DVDD18_IOLT	OFF	I
		TP_GPIO6_AO	DIO	1					
		SPIM4_MOSI	DIO	2					
		HDMITX20_SCL	DIO	7					
GPIO15	U32	GPIO15	DIO	0	0		DVDD18_IOLT	OFF	I
		TP_GPIO7_AO	DIO	1					
		SPIM4_MISO	DIO	2					
		HDMITX20_SDA	DIO	7					

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Ball name	Ball location	Signal name	Signal type	Aux. function	Reset function	Buffer type	Power domain	PU/PD reset	IO reset
GPIO16	AB32	GPIO16	DIO	0	0		DVDD18_IOLM	OFF	I
		TP_GPIO0_AO	DIO	1					
		UTXD3	DO	2					
		HDMITX20_PWR5V	DO	7					
GPIO17	AA35	GPIO17	DIO	0	0		DVDD18_IOLM	OFF	I
		TP_GPIO1_AO	DIO	1					
		URXD3	DI	2					
		CMFLASH2	DO	3					
		EDP_TX_HPD	DI	4					
		CMVREF7	DO	6					
CMMPDN0	G4	GPIO18	DIO	0	0		DVDD18_IORT	OFF	I
		TP_GPIO2_AO	DIO	1					
		CMFLASH0	DO	2					
		CMVREF4	DO	3					
		TDMIN_MCK	DIO	4					
		UTXD1	DO	5					
		TP_UTXD1_AO	DO	6					
CMMRST0	G3	GPIO19	DIO	0	0		DVDD18_IORT	OFF	I
		TP_GPIO3_AO	DIO	1					
		CMFLASH1	DO	2					
		CMVREF5	DO	3					
		TDMIN_BCK	DIO	4					
		URXD1	DI	5					
		TP_URXD1_AO	DI	6					

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Ball name	Ball location	Signal name	Signal type	Aux. function	Reset function	Buffer type	Power domain	PU/PD reset	IO reset
CMMPDN1	E3	GPIO20	DIO	0	0		DVDD18_IORT	OFF	I
		TP_GPIO4_AO	DIO	1					
		CMFLASH2	DO	2					
		CLKM2	DO	3					
		TDMIN_LRCK	DIO	4					
		URTS1	DO	5					
		TP_URTS1_AO	DO	6					
CMMRST1	G5	GPIO21	DIO	0	0		DVDD18_IORT	OFF	I
		TP_GPIO5_AO	DIO	1					
		CMFLASH3	DO	2					
		CLKM3	DO	3					
		TDMIN_DI	DI	4					
		UCTS1	DI	5					
		TP_UCTS1_AO	DI	6					
CMMCLK0	E4	GPIO22	DIO	0	0		DVDD18_IORT	OFF	I
		CMMCLK0	DO	1					
		TP_GPIO6_AO	DIO	5					
CMMCLK1	E5	GPIO23	DIO	0	0		DVDD18_IORT	OFF	I
		CMMCLK1	DO	1					
		PWM_2	DO	3					
		TP_GPIO7_AO	DIO	5					
		DP_TX_HPD	DI	6					

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Ball name	Ball location	Signal name	Signal type	Aux. function	Reset function	Buffer type	Power domain	PU/PD reset	IO reset
CMMCLK2	F4	GPIO24	DIO	0	0		DVDD18_IORT	OFF	I
		CMMCLK2	DO	1					
		PWM_3	DO	3					
		EDP_TX_HPD	DI	6					
DSI0_LCM_RST	Y9	GPIO25	DIO	0	0		DVDD18_IORM	OFF	I
		LCM_RST	DO	1					
		LCM1_RST	DO	2					
		DP_TX_HPD	DI	3					
DSI0_DSI_TE	AA7	GPIO26	DIO	0	0		DVDD18_IORM	OFF	I
		DSI_TE	DI	1					
		DSI1_TE	DI	2					
		EDP_TX_HPD	DI	3					
DSI1_LCM_RST	AA11	GPIO27	DIO	0	0		DVDD18_IORM	OFF	I
		LCM1_RST	DO	1					
		LCM_RST	DO	2					
		DP_TX_HPD	DI	3					
		CMVREF2	DO	4					
		PWM_2	DO	6					
DSI1_DSI_TE	Y5	GPIO28	DIO	0	0		DVDD18_IORM	OFF	I
		DSI1_TE	DI	1					
		DSI_TE	DI	2					
		EDP_TX_HPD	DI	3					
		CMVREF3	DO	4					
		PWM_3	DO	6					

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Ball name	Ball location	Signal name	Signal type	Aux. function	Reset function	Buffer type	Power domain	PU/PD reset	IO reset
DISP_PWM0	AA9	GPIO29	DIO	0	0		DVDD18_IORM	OFF	I
		DISP_PWM0	DO	1					
		DISP_PWM1	DO	2					
DISP_PWM1	Y11	GPIO30	DIO	0	0		DVDD18_IORM	OFF	I
		DISP_PWM1	DO	1					
		DISP_PWM0	DO	2					
		CMFLASH3	DO	3					
		PWM_1	DO	4					
UART0_TXD	U2	GPIO31	DIO	0	1		DVDD18_IORM	PU	OH
		UTXD0	DO	1					
		TP_UTXD1_AO	DO	2					
		TP_UTXD2_AO	DO	4					
		SSPM_UTXD_AO	DO	7					
UART0_RXD	U3	GPIO32	DIO	0	1		DVDD18_IORM	PU	I
		URXD0	DI	1					
		TP_URXD1_AO	DI	2					
		TP_URXD2_AO	DI	4					
		SSPM_URXD_AO	DI	7					
UART1_TXD	V1	GPIO33	DIO	0	0		DVDD18_IORM	OFF	I
		UTXD1	DO	1					
		URTS2	DO	2					
		TP_UTXD1_AO	DO	4					

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Ball name	Ball location	Signal name	Signal type	Aux. function	Reset function	Buffer type	Power domain	PU/PD reset	IO reset
UART1_RXD	V2	GPIO34	DIO	0	0		DVDD18_IORM	OFF	I
		URXD1	DI	1					
		UCTS2	DI	2					
		TP_URXD1_AO	DI	4					
UART2_TXD	U4	GPIO35	DIO	0	0		DVDD18_IORM	OFF	I
		UTXD2	DO	1					
		URTS1	DO	2					
		TP_URTS1_AO	DO	4					
		TP_UTXD2_AO	DO	5					
UART2_RXD	U5	GPIO36	DIO	0	0		DVDD18_IORM	OFF	I
		URXD2	DI	1					
		UCTS1	DI	2					
		TP_UCTS1_AO	DI	4					
		TP_URXD2_AO	DI	5					
JTMS	T6	GPIO37	DIO	0	1		DVDD18_IORM	PU	I
JTCK	T5	GPIO38	DIO	0	1		DVDD18_IORM	OFF	I
JTDI	T4	GPIO39	DIO	0	1		DVDD18_IORM	PU	I
JTDO	T1	GPIO40	DIO	0	1		DVDD18_IORM	OFF	OL
JTRST	T2	GPIO41	DIO	0	1		DVDD18_IORM	PU	I
KPCOL0	H31	GPIO42	DIO	0	1		DVDD18_IOLT	PU	I
		KPCOL0	DIO	1					

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Ball name	Ball location	Signal name	Signal type	Aux. function	Reset function	Buffer type	Power domain	PU/PD reset	IO reset
KPCOL1	J31	GPIO43	DIO	0	0		DVDD18_IOLT	OFF	I
		KPCOL1	DIO	1					
		DP_TX_HPD	DI	2					
		CMFLASH2	DO	3					
KPROW0	J30	GPIO44	DIO	0	1		DVDD18_IOLT	OFF	OL
		KPROW0	DIO	1					
KPROW1	K30	GPIO45	DIO	0	0		DVDD18_IOLT	OFF	I
		KPROW1	DIO	1					
		EDP_TX_HPD	DI	2					
		CMFLASH3	DO	3					
		I2SIN_MCK	DIO	4					
DPTX_HPD	AB33	GPIO46	DIO	0	0		DVDD18_IOLM	OFF	I
		DP_TX_HPD	DI	1					
		PWM_0	DO	2					
		VBUSVALID_2P	DI	3					
PCIE_WAKE_N	AA4	GPIO47	DIO	0	0		DVDD18_IORM	OFF	I
		WAKEN	DI	1					
PCIE_PERESET_N	AA3	GPIO48	DIO	0	0		DVDD18_IORM	OFF	I
		PERSTN	DO	1					
PCIE_CLKREQ_N	AA1	GPIO49	DIO	0	0		DVDD18_IORM	OFF	I
		CLKREQN	DIO	1					
HDMITX_PWR5V	AB34	GPIO50	DIO	0	0		DVDD18_IOLM	OFF	I
		HDMITX20_PWR5V	DO	1					
		IDDIG_1P	DI	3					

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HDMITX_HTPLG	AC32	GPIO51	DIO	0	0		DVDD18_IOLM	OFF	I
		HDMITX20_HTPLG	DI	1					
		EDP_TX_HPD	DI	2					
		USB_DRVVBUS_1P	DO	3					
HDMITX_CEC	AC33	GPIO52	DIO	0	0		DVDD18_IOLM	OFF	I
		HDMITX20_CEC	DIO	1					
		VBUSVALID_1P	DI	3					
HDMITX_SCL	AD32	GPIO53	DIO	0	0		DVDD18_IOLM	OFF	I
		HDMITX20_SCL	DIO	1					
		IDDIG_2P	DI	3					
HDMITX_SDA	AD33	GPIO54	DIO	0	0		DVDD18_IOLM	OFF	I
		HDMITX20_SDA	DIO	1					
		USB_DRVVBUS_2P	DO	3					
SCL0	Y4	GPIO55	DIO	0	1		DVDD18_IORM	PU	I
		SCL0	DIO	1					
		SCP_SCL0	DIO	2					
		SCP_SCL1	DIO	3					
SDA0	W6	GPIO56	DIO	0	1		DVDD18_IORM	PU	I
		SDA0	DIO	1					
		SCP_SDA0	DIO	2					
		SCP_SDA1	DIO	3					
SCL1	M36	GPIO57	DIO	0	1		DVDD18_IOLT	PU	I
		SCL1	DIO	1					

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SDA1	L36	GPIO58	DIO	0	1		DVDD18_IOLT	PU	I
		SDA1	DIO	1					
SCL2	Y2	GPIO59	DIO	0	1		DVDD18_IORM	PU	I
		SCL2	DIO	1					
		SCP_SCL0	DIO	2					
		SCP_SCL1	DIO	3					
SDA2	AA2	GPIO60	DIO	0	1		DVDD18_IORM	PU	I
		SDA2	DIO	1					
		SCP_SDA0	DIO	2					
		SCP_SDA1	DIO	3					
SCL3	W2	GPIO61	DIO	0	1		DVDD18_IORM	PU	I
		SCL3	DIO	1					
		SCP_SCL0	DIO	2					
		SCP_SCL1	DIO	3					
SDA3	W1	GPIO62	DIO	0	1		DVDD18_IORM	PU	I
		SDA3	DIO	1					
		SCP_SDA0	DIO	2					
		SCP_SDA1	DIO	3					
SCL4	K36	GPIO63	DIO	0	1		DVDD18_IOLT	PU	I
		SCL4	DIO	1					
SDA4	K37	GPIO64	DIO	0	1		DVDD18_IOLT	PU	I
		SDA4	DIO	1					

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SCL5	F5	GPIO65	DIO	0	1		DVDD18_IORT	PU	I
		SCL5	DIO	1					
		SCP_SCL0	DIO	2					
		SCP_SCL1	DIO	3					
SDA5	F6	GPIO66	DIO	0	1		DVDD18_IORT	PU	I
		SDA5	DIO	1					
		SCP_SDA0	DIO	2					
		SCP_SDA1	DIO	3					
SCL6	H7	GPIO67	DIO	0	1		DVDD18_IORT	PU	I
		SCL6	DIO	1					
		SCP_SCL0	DIO	2					
		SCP_SCL1	DIO	3					
SDA6	G6	GPIO68	DIO	0	1		DVDD18_IORT	PU	I
		SDA6	DIO	1					
		SCP_SDA0	DIO	2					
		SCP_SDA1	DIO	3					
SPIM0_CSB	V6	GPIO69	DIO	0	0		DVDD18_IORM	OFF	I
		SPIM0_CSB	DO	1					
		SCP_SPI0_CS	DO	2					
		DMIC3_CLK	DO	3					
		CMVREF0	DO	5					

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SPIM0_CLK	T11	GPIO70	DIO	0	0		DVDD18_IORM	OFF	I
		SPIM0_CLK	DO	1					
		SCP_SPI0_CK	DO	2					
		DMIC3_DAT	DI	3					
		CMVREF1	DO	5					
SPIM0_MOSI	V7	GPIO71	DIO	0	0		DVDD18_IORM	OFF	I
		SPIM0_MOSI	DIO	1					
		SCP_SPI0_MO	DO	2					
		DMIC3_DAT_R	DI	3					
		CMVREF2	DO	5					
SPIM0_MISO	V8	GPIO72	DIO	0	0		DVDD18_IORM	OFF	I
		SPIM0_MISO	DIO	1					
		SCP_SPI0_MI	DI	2					
		DMIC4_CLK	DO	3					
		CMVREF3	DO	5					
SPIM0_MIO2	U7	GPIO73	DIO	0	0		DVDD18_IORM	OFF	I
		SPIM0_MIO2	DIO	1					
		UTXD3	DO	2					
		DMIC4_DAT	DI	3					
		CLKM0	DO	4					
		CMVREF4	DO	5					

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SPIM0_MIO3	U8	GPIO74	DIO	0	0		DVDD18_IORM	OFF	I
		SPIM0_MIO3	DIO	1					
		URXD3	DI	2					
		DMIC4_DAT_R	DI	3					
		CLKM1	DO	4					
		CMVREF5	DO	5					
SPIM1_CSB	T9	GPIO75	DIO	0	0		DVDD18_IORM	OFF	I
		SPIM1_CSB	DO	1					
		SCP_SPI1_A_CS	DO	2					
		TDMIN_MCK	DIO	3					
		SCP_SCL0	DIO	4					
		CMVREF6	DO	5					
SPIM1_CLK	T10	GPIO76	DIO	0	0		DVDD18_IORM	OFF	I
		SPIM1_CLK	DO	1					
		SCP_SPI1_A_CK	DO	2					
		TDMIN_BCK	DIO	3					
		SCP_SDA0	DIO	4					
		CMVREF7	DO	5					
SPIM1_MOSI	T8	GPIO77	DIO	0	0		DVDD18_IORM	OFF	I
		SPIM1_MOSI	DIO	1					
		SCP_SPI1_A_MO	DO	2					
		TDMIN_LRCK	DIO	3					
		SCP_SCL1	DIO	4					

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SPIM1_MISO	T7	GPIO78	DIO	0	0		DVDD18_IORM	OFF	I
		SPIM1_MISO	DIO	1					
		SCP_SPI1_A_MI	DI	2					
		TDMIN_DI	DI	3					
		SCP_SDA1	DIO	4					
SPIM2_CSB	G2	GPIO79	DIO	0	0		DVDD18_IORT	OFF	I
		SPIM2_CSB	DO	1					
		SCP_SPI2_CS	DO	2					
		I2SO1_MCK	DO	3					
		UTXD2	DO	4					
		TP_UTXD2_AO	DO	5					
		PCM_SYNC	DIO	6					
SPIM2_CLK	G1	GPIO80	DIO	0	0		DVDD18_IORT	OFF	I
		SPIM2_CLK	DO	1					
		SCP_SPI2_CK	DO	2					
		I2SO1_BCK	DO	3					
		URXD2	DI	4					
		TP_URXD2_AO	DI	5					
		PCM_CLK	DIO	6					

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SPIM2_MOSI	F2	GPIO81	DIO	0	0		DVDD18_IORT	OFF	I
		SPIM2_MOSI	DIO	1					
		SCP_SPI2_MO	DO	2					
		I2SO1_WS	DO	3					
		URTS2	DO	4					
		TP_URTS2_AO	DO	5					
		PCM_DO	DO	6					
SPIM2_MISO	E2	GPIO82	DIO	0	0		DVDD18_IORT	OFF	I
		SPIM2_MISO	DIO	1					
		SCP_SPI2_MI	DI	2					
		I2SO1_D0	DO	3					
		UCTS2	DI	4					
		TP_UCTS2_AO	DI	5					
		PCM_DI	DI	6					
USB0_IDDIG	R36	GPIO83	DIO	0	0		DVDD18_IOLT	OFF	I
		IDDIG	DI	1					
USB0_DRV_VBUS	P36	GPIO84	DIO	0	0		DVDD18_IOLT	OFF	I
		USB_DRVVBUS	DO	1					
USB0_VBUS_VALID	P34	GPIO85	DIO	0	0		DVDD18_IOLT	OFF	I
		VBUSVALID	DI	1					

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USB1_IDDIG	R34	GPIO86	DIO	0	0		DVDD18_IOLT	OFF	I
		IDDIG_1P	DI	1					
		UTXD1	DO	2					
		URTS2	DO	3					
		PWM_2	DO	4					
		TP_GPIO4_AO	DIO	5					
		AUXIF_ST0	DO	6					
USB1_DRV_VBUS	R33	GPIO87	DIO	0	0		DVDD18_IOLT	OFF	I
		USB_DRVVBUS_1P	DO	1					
		URXD1	DI	2					
		UCTS2	DI	3					
		PWM_3	DO	4					
		TP_GPIO5_AO	DIO	5					
		AUXIF_CLK0	DO	6					
USB1_VBUS_VALID	T33	GPIO88	DIO	0	0		DVDD18_IOLT	OFF	I
		VBUSVALID_1P	DI	1					
		UTXD2	DO	2					
		URTS1	DO	3					
		CLKM2	DO	4					
		TP_GPIO6_AO	DIO	5					
		AUXIF_ST1	DO	6					

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USB2_IDDIG	P31	GPIO89	DIO	0	0		DVDD18_IOLT	OFF	I
		IDDIG_2P	DI	1					
		URXD2	DI	2					
		UCTS1	DI	3					
		CLKM3	DO	4					
		TP_GPIO7_AO	DIO	5					
		AUXIF_CLK1	DO	6					
USB2_DRV_VBUS	P32	GPIO90	DIO	0	0		DVDD18_IOLT	OFF	I
		USB_DRVVBUS_2P	DO	1					
		UTXD3	DO	2					
USB2_VBUS_VALID	R30	GPIO91	DIO	0	0		DVDD18_IOLT	OFF	I
		VBUSVALID_2P	DI	1					
		URXD3	DI	2					
PWRAP_SPI_CSN	K32	GPIO92	DIO	0	1		DVDD18_IOLT	PU	OH
		PWRAP_SPI0_CSN	DO	1					
PWRAP_SPI_CK	K31	GPIO93	DIO	0	1		DVDD18_IOLT	OFF	OL
		PWRAP_SPI0_CK	DO	1					
PWRAP_SPI_MO	L30	GPIO94	DIO	0	1		DVDD18_IOLT	OFF	I
		PWRAP_SPI0_MO	DIO	1					
		PWRAP_SPI0_MI	DIO	2					
PWRAP_SPI_MI	L31	GPIO95	DIO	0	1		DVDD18_IOLT	OFF	I
		PWRAP_SPI0_MI	DIO	1					
		PWRAP_SPI0_MO	DIO	2					

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PMIC_SRCLKENA0	L33	GPIO96	DIO	0	1		DVDD18_IOLT	PU	OH
		SRCLKENA0	DO	1					
PMIC_SRCLKENA1	L34	GPIO97	DIO	0	1		DVDD18_IOLT	PU	OH
		SRCLKENA1	DO	1					
SCP_VREQ_VAO	M31	GPIO98	DIO	0	0		DVDD18_IOLT	OFF	I
		SCP_VREQ_VAO	DO	1					
PMIC_RTC32K_CK	N37	GPIO99	DIO	0	1		DVDD18_IOLT	OFF	I
		RTC32K_CK	DI	1					
PMIC_WATCHDOG	K34	GPIO100	DIO	0	1		DVDD18_IOLT	OFF	OL
		WATCHDOG	DO	1					
AUD_CLK_MOSI	M33	GPIO101	DIO	0	0		DVDD18_IOLT	OFF	I
		AUD_CLK_MOSI	DO	1					
		I2SO1_MCK	DO	2					
		I2SIN_BCK	DIO	3					
AUD_SYNC_MOSI	M35	GPIO102	DIO	0	0		DVDD18_IOLT	OFF	I
		AUD_SYNC_MOSI	DO	1					
		I2SO1_BCK	DO	2					
		I2SIN_WS	DIO	3					
AUD_DAT_MOSI0	M34	GPIO103	DIO	0	0		DVDD18_IOLT	OFF	I
		AUD_DAT_MOSI0	DO	1					
		I2SO1_WS	DO	2					
		I2SIN_D0	DI	3					

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AUD_DAT_MOSI1	N33	GPIO104	DIO	0	0		DVDD18_IOLT	OFF	I
		AUD_DAT_MOSI1	DO	1					
		I2SO1_D0	DO	2					
		I2SIN_D1	DI	3					
AUD_DAT_MISO0	M30	GPIO105	DIO	0	0		DVDD18_IOLT	OFF	I
		AUD_DAT_MISO0	DI	1					
		VOW_DAT_MISO	DI	2					
		I2SIN_D2	DI	3					
AUD_DAT_MISO1	M32	GPIO106	DIO	0	0		DVDD18_IOLT	OFF	I
		AUD_DAT_MISO1	DI	1					
		VOW_CLK_MISO	DI	2					
		I2SIN_D3	DI	3					
I2SIN_MCK	G36	GPIO107	DIO	0	0		DVDD18_IOLT	OFF	I
		I2SIN_MCK	DIO	1					
		SPLIN_MCK	DI	2					
		SPDIF_IN0	DI	3					
		CMVREF4	DO	4					
		AUXIF_ST0	DO	5					
I2SIN_BCK	H36	GPIO108	DIO	0	0		DVDD18_IOLT	OFF	I
		I2SIN_BCK	DIO	1					
		SPLIN_LRCK	DI	2					
		DMIC4_CLK	DO	3					
		CMVREF5	DO	4					
		AUXIF_CLK0	DO	5					

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I2SIN_WS	J36	GPIO109	DIO	0	0		DVDD18_IOLT	OFF	I
		I2SIN_WS	DIO	1					
		SPLIN_BCK	DI	2					
		DMIC4_DAT	DI	3					
		CMVREF6	DO	4					
		AUXIF_ST1	DO	5					
I2SIN_D0	J37	GPIO110	DIO	0	0		DVDD18_IOLT	OFF	I
		I2SIN_D0	DI	1					
		SPLIN_D0	DI	2					
		DMIC4_DAT_R	DI	3					
		CMVREF7	DO	4					
		AUXIF_CLK1	DO	5					
I2SIN_D1	G33	GPIO111	DIO	0	0		DVDD18_IOLT	OFF	I
		I2SIN_D1	DI	1					
		SPLIN_D1	DI	2					
		DMIC3_CLK	DO	3					
		SPDIF_OUT	DO	4					
I2SIN_D2	G32	GPIO112	DIO	0	0		DVDD18_IOLT	OFF	I
		I2SIN_D2	DI	1					
		SPLIN_D2	DI	2					
		DMIC3_DAT	DI	3					
		TDMIN_MCK	DIO	4					
		I2SO1_WS	DO	5					

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I2SIN_D3	H35	GPIO113	DIO	0	0		DVDD18_IOLT	OFF	I
		I2SIN_D3	DI	1					
		SPLIN_D3	DI	2					
		DMIC3_DAT_R	DI	3					
		TDMIN_BCK	DIO	4					
		I2SO1_D0	DO	5					
I2SO2_MCK	H34	GPIO114	DIO	0	0		DVDD18_IOLT	OFF	I
		I2SO2_MCK	DO	1					
		I2SIN_MCK	DIO	2					
I2SO2_BCK	H33	GPIO115	DIO	0	0		DVDD18_IOLT	OFF	I
		I2SO2_BCK	DIO	1					
		I2SIN_BCK	DIO	2					
I2SO2_WS	J34	GPIO116	DIO	0	0		DVDD18_IOLT	OFF	I
		I2SO2_WS	DIO	1					
		I2SIN_WS	DIO	2					
I2SO2_D0	J33	GPIO117	DIO	0	0		DVDD18_IOLT	OFF	I
		I2SO2_D0	DO	1					
		I2SIN_D0	DI	2					
I2SO2_D1	G31	GPIO118	DIO	0	0		DVDD18_IOLT	OFF	I
		I2SO2_D1	DO	1					
		I2SIN_D1	DI	2					

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I2SO2_D2	G30	GPIO119	DIO	0	0		DVDD18_IOLT	OFF	I
		I2SO2_D2	DO	1					
		I2SIN_D2	DI	2					
		UTXD3	DO	3					
		TDMIN_LRCK	DIO	4					
		I2SO1_MCK	DO	5					
I2SO2_D3	H32	GPIO120	DIO	0	0		DVDD18_IOLT	OFF	I
		I2SO2_D3	DO	1					
		I2SIN_D3	DI	2					
		URXD3	DI	3					
		TDMIN_DI	DI	4					
		I2SO1_BCK	DO	5					
PCM_CLK	AD30	GPIO121	DIO	0	0		DVDD18_IOLM	OFF	I
		PCM_CLK	DIO	1					
		SPIM4_CSB	DO	2					
		SCP_SPI1_B_CS	DO	3					
		TP_UTXD2_AO	DO	4					
		AUXIF_ST0	DO	5					
PCM_SYNC	AC31	GPIO122	DIO	0	0		DVDD18_IOLM	OFF	I
		PCM_SYNC	DIO	1					
		SPIM4_CLK	DO	2					
		SCP_SPI1_B_CK	DO	3					
		TP_URXD2_AO	DI	4					
		AUXIF_CLK0	DO	5					

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PCM_DO	AC30	GPIO123	DIO	0	0		DVDD18_IOLM	OFF	I
		PCM_DO	DO	1					
		SPIM4_MOSI	DIO	2					
		SCP_SPI1_B_MO	DO	3					
		TP_URTS2_AO	DO	4					
		AUXIF_ST1	DO	5					
PCM_DI	AB31	GPIO124	DIO	0	0		DVDD18_IOLM	OFF	I
		PCM_DI	DI	1					
		SPIM4_MISO	DIO	2					
		SCP_SPI1_B_MI	DI	3					
		TP_UCTS2_AO	DI	4					
		AUXIF_CLK1	DO	5					
DMIC1_CLK	N30	GPIO125	DIO	0	0		DVDD18_IOLT	OFF	I
		DMIC1_CLK	DO	1					
		SPINOR_CK	DO	2					
		TDMIN_MCK	DIO	3					
		LVTS_FOUT	DO	6					
DMIC1_DAT	N31	GPIO126	DIO	0	0		DVDD18_IOLT	OFF	I
		DMIC1_DAT	DI	1					
		SPINOR_CS	DO	2					
		TDMIN_BCK	DIO	3					
		LVTS_SDO	DO	6					

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Ball name	Ball location	Signal name	Signal type	Aux. function	Reset function	Buffer type	Power domain	PU/PD reset	IO reset
DMIC1_DAT_R	P30	GPIO127	DIO	0	0		DVDD18_IOLT	OFF	I
		DMIC1_DAT_R	DI	1					
		SPINOR_IO0	DIO	2					
		TDMIN_LRCK	DIO	3					
		LVTS_26M	DI	6					
DMIC2_CLK	N34	GPIO128	DIO	0	0		DVDD18_IOLT	OFF	I
		DMIC2_CLK	DO	1					
		SPINOR_IO1	DIO	2					
		TDMIN_DI	DI	3					
		LVTS_SCF	DI	6					
DMIC2_DAT	P33	GPIO129	DIO	0	0		DVDD18_IOLT	OFF	I
		DMIC2_DAT	DI	1					
		SPINOR_IO2	DIO	2					
		SPDIF_IN1	DI	3					
		LVTS_SCK	DI	6					
DMIC2_DAT_R	P35	GPIO130	DIO	0	0		DVDD18_IOLT	OFF	I
		DMIC2_DAT_R	DI	1					
		SPINOR_IO3	DIO	2					
		SPDIF_IN2	DI	3					
		LVTS_SDI	DI	6					

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DPI_D0	AB9	GPIO131	DIO	0	0		DVDD28_IODPI	OFF	I
		DPI_D0	DO	1					
		GBE_TXD3	DO	2					
		DMIC1_CLK	DO	3					
		I2SO2_MCK	DO	4					
		TP_GPIO0_AO	DIO	5					
		SPIM5_CSB	DO	6					
DPI_D1	AC9	GPIO132	DIO	0	0		DVDD28_IODPI	OFF	I
		DPI_D1	DO	1					
		GBE_TXD2	DO	2					
		DMIC1_DAT	DI	3					
		I2SO2_BCK	DIO	4					
		TP_GPIO1_AO	DIO	5					
		SPIM5_CLK	DO	6					
DPI_D2	AB8	GPIO133	DIO	0	0		DVDD28_IODPI	OFF	I
		DPI_D2	DO	1					
		GBE_TXD1	DO	2					
		DMIC1_DAT_R	DI	3					
		I2SO2_WS	DIO	4					
		TP_GPIO2_AO	DIO	5					
		SPIM5_MOSI	DIO	6					

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DPI_D3	AC4	GPIO134	DIO	0	0		DVDD28_IODPI	OFF	I
		DPI_D3	DO	1					
		GBE_TXD0	DO	2					
		DMIC2_CLK	DO	3					
		I2SO2_D0	DO	4					
		TP_GPIO3_AO	DIO	5					
		SPIM5_MISO	DIO	6					
DPI_D4	AB3	GPIO135	DIO	0	0		DVDD28_IODPI	OFF	I
		DPI_D4	DO	1					
		GBE_RXD3	DI	2					
		DMIC2_DAT	DI	3					
		I2SO2_D1	DO	4					
		TP_GPIO4_AO	DIO	5					
		WAKEN	DI	6					
DPI_D5	AA8	GPIO136	DIO	0	0		DVDD28_IODPI	OFF	I
		DPI_D5	DO	1					
		GBE_RXD2	DI	2					
		DMIC2_DAT_R	DI	3					
		I2SO2_D2	DO	4					
		TP_GPIO5_AO	DIO	5					
		PERSTN	DO	6					

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DPI_D6	AC8	GPIO137	DIO	0	0		DVDD28_IODPI	OFF	I
		DPI_D6	DO	1					
		GBE_RXD1	DI	2					
		DMIC3_CLK	DO	3					
		I2SO2_D3	DO	4					
		TP_GPIO6_AO	DIO	5					
		CLKREQN	DIO	6					
		PWM_0	DO	7					
DPI_D7	AB7	GPIO138	DIO	0	0		DVDD28_IODPI	OFF	I
		DPI_D7	DO	1					
		GBE_RXD0	DI	2					
		DMIC3_DAT	DI	3					
		CLKM2	DO	4					
		TP_GPIO7_AO	DIO	5					
DPI_D8	AB6	GPIO139	DIO	0	0		DVDD28_IODPI	OFF	I
		DPI_D8	DO	1					
		GBE_TXC	DIO	2					
		DMIC3_DAT_R	DI	3					
		CLKM3	DO	4					
		TP_UTXD2_AO	DO	5					
		UTXD2	DO	6					

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DPI_D9	AB5	GPIO140	DIO	0	0		DVDD28_IODPI	OFF	I
		DPI_D9	DO	1					
		GBE_RXC	DI	2					
		DMIC4_CLK	DO	3					
		PWM_2	DO	4					
		TP_URXD2_AO	DI	5					
		URXD2	DI	6					
DPI_D10	AC5	GPIO141	DIO	0	0		DVDD28_IODPI	OFF	I
		DPI_D10	DO	1					
		GBE_RXDV	DI	2					
		DMIC4_DAT	DI	3					
		PWM_3	DO	4					
		TP_URTS2_AO	DO	5					
		URTS2	DO	6					
DPI_D11	AA5	GPIO142	DIO	0	0		DVDD28_IODPI	OFF	I
		DPI_D11	DO	1					
		GBE_TXEN	DO	2					
		DMIC4_DAT_R	DI	3					
		PWM_1	DO	4					
		TP_UCTS2_AO	DI	5					
		UCTS2	DI	6					

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DPI_D12	AA6	GPIO143	DIO	0	0		DVDD28_IODPI	OFF	I
		DPI_D12	DO	1					
		GBE_MDC	DO	2					
		CLKM0	DO	4					
		SPIM3_CSB	DO	5					
		UTXD1	DO	6					
DPI_D13	AC6	GPIO144	DIO	0	0		DVDD28_IODPI	OFF	I
		DPI_D13	DO	1					
		GBE_MDIO	DIO	2					
		CLKM1	DO	4					
		SPIM3_CLK	DO	5					
		URXD1	DI	6					
DPI_D14	AC7	GPIO145	DIO	0	0		DVDD28_IODPI	OFF	I
		DPI_D14	DO	1					
		GBE_TXER	DO	2					
		CMFLASH0	DO	4					
		SPIM3_MOSI	DIO	5					
		GBE_AUX_PPS2	DIO	6					
DPI_D15	AB4	GPIO146	DIO	0	0		DVDD28_IODPI	OFF	I
		DPI_D15	DO	1					
		GBE_RXER	DI	2					
		CMFLASH1	DO	4					
		SPIM3_MISO	DIO	5					
		GBE_AUX_PPS3	DIO	6					

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DPI_HSYNC	AD11	GPIO147	DIO	0	0		DVDD28_IODPI	OFF	I
		DPI_HSYNC	DO	1					
		GBE_COL	DI	2					
		I2SO1_MCK	DO	3					
		CMVREF0	DO	4					
		SPDIF_OUT	DO	5					
		URTS1	DO	6					
DPI_VSYNC	AD10	GPIO148	DIO	0	0		DVDD28_IODPI	OFF	I
		DPI_VSYNC	DO	1					
		GBE_INTR	DI	2					
		I2SO1_BCK	DO	3					
		CMVREF1	DO	4					
		SPDIF_IN0	DI	5					
		UCTS1	DI	6					
DPI_DE	AB2	GPIO149	DIO	0	0		DVDD28_IODPI	OFF	I
		DPI_DE	DO	1					
		GBE_AUX_PPS0	DIO	2					
		I2SO1_WS	DO	3					
		CMVREF2	DO	4					
		SPDIF_IN1	DI	5					
		UTXD3	DO	6					

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DPI_CK	AB1	GPIO150	DIO	0	0		DVDD28_IODPI	OFF	I
		DPI_CK	DO	1					
		GBE_AUX_PPS1	DIO	2					
		I2SO1_D0	DO	3					
		CMVREF3	DO	4					
		SPDIF_IN2	DI	5					
		URXD3	DI	6					
EMMC_DAT7	D37	GPIO151	DIO	0	1		DVDD18_IOEMMC	PU	I
		MSDC0_DAT7	DIO	1					
EMMC_DAT6	E36	GPIO152	DIO	0	1		DVDD18_IOEMMC	PU	I
		MSDC0_DAT6	DIO	1					
EMMC_DAT5	F37	GPIO153	DIO	0	1		DVDD18_IOEMMC	PU	I
		MSDC0_DAT5	DIO	1					
EMMC_DAT4	D35	GPIO154	DIO	0	1		DVDD18_IOEMMC	PU	I
		MSDC0_DAT4	DIO	1					
EMMC_RSTB	E34	GPIO155	DIO	0	1		DVDD18_IOEMMC	PU	OH
		MSDC0_RSTB	DO	1					
EMMC_CMD	F33	GPIO156	DIO	0	1		DVDD18_IOEMMC	PU	I
		MSDC0_CMD	DIO	1					
EMMC_CLK	F32	GPIO157	DIO	0	1		DVDD18_IOEMMC	OFF	OL
		MSDC0_CLK	DO	1					
EMMC_DAT3	E32	GPIO158	DIO	0	1		DVDD18_IOEMMC	PU	I
		MSDC0_DAT3	DIO	1					

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EMMC_DAT2	D36	GPIO159	DIO	0	1		DVDD18_IOEMMC	PU	I
		MSDC0_DAT2	DIO	1					
EMMC_DAT1	F36	GPIO160	DIO	0	1		DVDD18_IOEMMC	PU	I
		MSDC0_DAT1	DIO	1					
EMMC_DAT0	D33	GPIO161	DIO	0	1		DVDD18_IOEMMC	PU	I
		MSDC0_DAT0	DIO	1					
EMMC_DSL	E35	GPIO162	DIO	0	1		DVDD18_IOEMMC	OFF	I
		MSDC0_DSL	DI	1					
MSDC1_CMD	D3	GPIO163	DIO	0	0		DVDD28_MSDC1	OFF	I
		MSDC1_CMD	DIO	1					
		SPDIF_OUT	DO	2					
MSDC1_CLK	D4	GPIO164	DIO	0	0		DVDD28_MSDC1	OFF	I
		MSDC1_CLK	DO	1					
		SPDIF_IN0	DI	2					
MSDC1_DAT0	D2	GPIO165	DIO	0	0		DVDD28_MSDC1	OFF	I
		MSDC1_DAT0	DIO	1					
		SPDIF_IN1	DI	2					
MSDC1_DAT1	D1	GPIO166	DIO	0	0		DVDD28_MSDC1	OFF	I
		MSDC1_DAT1	DIO	1					
		SPDIF_IN2	DI	2					
MSDC1_DAT2	C4	GPIO167	DIO	0	0		DVDD28_MSDC1	OFF	I
		MSDC1_DAT2	DIO	1					
		PWM_0	DO	2					

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MSDC1_DAT3	C3	GPIO168	DIO	0	0		DVDD28_MSDC1	OFF	I
		MSDC1_DAT3	DIO	1					
		PWM_1	DO	2					
		CLKM0	DO	3					
MSDC2_CMD	AC35	GPIO169	DIO	0	0		DVDD28_MSDC2	OFF	I
		MSDC2_CMD	DIO	1					
		LVTS_FOUT	DO	2					
		TDMIN_MCK	DIO	6					
MSDC2_CLK	AD35	GPIO170	DIO	0	0		DVDD28_MSDC2	OFF	I
		MSDC2_CLK	DO	1					
		LVTS_SDO	DO	2					
		TDMIN_BCK	DIO	6					
MSDC2_DAT0	AD37	GPIO171	DIO	0	0		DVDD28_MSDC2	OFF	I
		MSDC2_DAT0	DIO	1					
		LVTS_26M	DI	2					
		TDMIN_LRCK	DIO	6					
MSDC2_DAT1	AD36	GPIO172	DIO	0	0		DVDD28_MSDC2	OFF	I
		MSDC2_DAT1	DIO	1					
		LVTS_SCF	DI	2					
		TDMIN_DI	DI	6					
MSDC2_DAT2	AB37	GPIO173	DIO	0	0		DVDD28_MSDC2	OFF	I
		MSDC2_DAT2	DIO	1					
		LVTS_SCK	DI	2					

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MSDC2_DAT3	AB35	GPIO174	DIO	0	0		DVDD28_MSDC2	OFF	I
		MSDC2_DAT3	DIO	1					
		LVTS_SDI	DI	2					
SPMI_M_SCL	K33	GPIO175	DIO	0	1		DVDD18_IOLT	OFF	OL
		SPMI_M_SCL	DIO	1					
SPMI_M_SDA	K35	GPIO176	DIO	0	1		DVDD18_IOLT	OFF	I
		SPMI_M_SDA	DIO	1					
SYSRSTB	T32	SYSRSTB	DI				DVDD18_IOLT		
TESTMODE	T34	TESTMODE	DI				DVDD18_IOLT		
X26M_IN	AE34	X26M_IN	AI				AVDD12_CKSQ		
EMI0_CA0	AT22	EMI0_CA0	DO			DDRIO	AVDDQ_EMI		
EMI0_CA1	AR22	EMI0_CA1	DO			DDRIO	AVDDQ_EMI		
EMI0_CA2	AM23	EMI0_CA2	DO			DDRIO	AVDDQ_EMI		
EMI0_CA3	AM22	EMI0_CA3	DO			DDRIO	AVDDQ_EMI		
EMI0_CA4	AN21	EMI0_CA4	DO			DDRIO	AVDDQ_EMI		
EMI0_CA5	AP21	EMI0_CA5	DO			DDRIO	AVDDQ_EMI		
EMI0_CK_C	AL20	EMI0_CK_C	DO			DDRIO	AVDDQ_EMI		
EMI0_CK_T	AM20	EMI0_CK_T	DO			DDRIO	AVDDQ_EMI		
EMI0_CKE0	AU20	EMI0_CKE0	DO			DDRIO	AVDDQ_EMI		
EMI0_CKE1	AT20	EMI0_CKE1	DO			DDRIO	AVDDQ_EMI		
EMI0_CS0	AR20	EMI0_CS0	DO			DDRIO	AVDDQ_EMI		
EMI0_CS1	AU22	EMI0_CS1	DO			DDRIO	AVDDQ_EMI		
EMI0_DMI0	AU25	EMI0_DMI0	DIO			DDRIO	AVDDQ_EMI		
EMI0_DMI1	AU31	EMI0_DMI1	DIO			DDRIO	AVDDQ_EMI		
EMI0_DQ0	AU27	EMI0_DQ0	DIO			DDRIO	AVDDQ_EMI		
EMI0_DQ1	AT26	EMI0_DQ1	DIO			DDRIO	AVDDQ_EMI		
EMI0_DQ10	AP30	EMI0_DQ10	DIO			DDRIO	AVDDQ_EMI		

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EMI0_DQ11	AN29	EMI0_DQ11	DIO			DDRIO	AVDDQ_EMI		
EMI0_DQ12	AR29	EMI0_DQ12	DIO			DDRIO	AVDDQ_EMI		
EMI0_DQ13	AP31	EMI0_DQ13	DIO			DDRIO	AVDDQ_EMI		
EMI0_DQ14	AT30	EMI0_DQ14	DIO			DDRIO	AVDDQ_EMI		
EMI0_DQ15	AU29	EMI0_DQ15	DIO			DDRIO	AVDDQ_EMI		
EMI0_DQ2	AL25	EMI0_DQ2	DIO			DDRIO	AVDDQ_EMI		
EMI0_DQ3	AP25	EMI0_DQ3	DIO			DDRIO	AVDDQ_EMI		
EMI0_DQ4	AL24	EMI0_DQ4	DIO			DDRIO	AVDDQ_EMI		
EMI0_DQ5	AN25	EMI0_DQ5	DIO			DDRIO	AVDDQ_EMI		
EMI0_DQ6	AT24	EMI0_DQ6	DIO			DDRIO	AVDDQ_EMI		
EMI0_DQ7	AT28	EMI0_DQ7	DIO			DDRIO	AVDDQ_EMI		
EMI0_DQ8	AU34	EMI0_DQ8	DIO			DDRIO	AVDDQ_EMI		
EMI0_DQ9	AN31	EMI0_DQ9	DIO			DDRIO	AVDDQ_EMI		
EMI0_DQS0_C	AN27	EMI0_DQS0_C	DIO			DDRIO	AVDDQ_EMI		
EMI0_DQS0_T	AM27	EMI0_DQS0_T	DIO			DDRIO	AVDDQ_EMI		
EMI0_DQS1_C	AR32	EMI0_DQS1_C	DIO			DDRIO	AVDDQ_EMI		
EMI0_DQS1_T	AT32	EMI0_DQS1_T	DIO			DDRIO	AVDDQ_EMI		
EMI0_EXTR	AT2	EMI0_EXTR	AIO			DDRIO	AVDDQ_EMI		
EMI0_RESET_N	AU35	EMI0_RESET_N	DO			DDRIO	AVDDQ_EMI		
EMI0_TP	AR3	EMI0_TP	AIO			DDRIO	AVDDQ_EMI		
EMI1_CA0	AT16	EMI1_CA0	DO			DDRIO	AVDDQ_EMI		
EMI1_CA1	AR16	EMI1_CA1	DO			DDRIO	AVDDQ_EMI		
EMI1_CA2	AL15	EMI1_CA2	DO			DDRIO	AVDDQ_EMI		
EMI1_CA3	AP16	EMI1_CA3	DO			DDRIO	AVDDQ_EMI		
EMI1_CA4	AN16	EMI1_CA4	DO			DDRIO	AVDDQ_EMI		
EMI1_CA5	AL16	EMI1_CA5	DO			DDRIO	AVDDQ_EMI		
EMI1_CK_C	AL18	EMI1_CK_C	DO			DDRIO	AVDDQ_EMI		

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EMI1_CK_T	AM18	EMI1_CK_T	DO			DDRIO	AVDDQ_EMI		
EMI1_CKE0	AU18	EMI1_CKE0	DO			DDRIO	AVDDQ_EMI		
EMI1_CKE1	AT18	EMI1_CKE1	DO			DDRIO	AVDDQ_EMI		
EMI1_CS0	AR18	EMI1_CS0	DO			DDRIO	AVDDQ_EMI		
EMI1_CS1	AU16	EMI1_CS1	DO			DDRIO	AVDDQ_EMI		
EMI1_DMI0	AU13	EMI1_DMI0	DIO			DDRIO	AVDDQ_EMI		
EMI1_DMI1	AU7	EMI1_DMI1	DIO			DDRIO	AVDDQ_EMI		
EMI1_DQ0	AU11	EMI1_DQ0	DIO			DDRIO	AVDDQ_EMI		
EMI1_DQ1	AT12	EMI1_DQ1	DIO			DDRIO	AVDDQ_EMI		
EMI1_DQ10	AN8	EMI1_DQ10	DIO			DDRIO	AVDDQ_EMI		
EMI1_DQ11	AR9	EMI1_DQ11	DIO			DDRIO	AVDDQ_EMI		
EMI1_DQ12	AN9	EMI1_DQ12	DIO			DDRIO	AVDDQ_EMI		
EMI1_DQ13	AR6	EMI1_DQ13	DIO			DDRIO	AVDDQ_EMI		
EMI1_DQ14	AT8	EMI1_DQ14	DIO			DDRIO	AVDDQ_EMI		
EMI1_DQ15	AU9	EMI1_DQ15	DIO			DDRIO	AVDDQ_EMI		
EMI1_DQ2	AR11	EMI1_DQ2	DIO			DDRIO	AVDDQ_EMI		
EMI1_DQ3	AN13	EMI1_DQ3	DIO			DDRIO	AVDDQ_EMI		
EMI1_DQ4	AL13	EMI1_DQ4	DIO			DDRIO	AVDDQ_EMI		
EMI1_DQ5	AP13	EMI1_DQ5	DIO			DDRIO	AVDDQ_EMI		
EMI1_DQ6	AT14	EMI1_DQ6	DIO			DDRIO	AVDDQ_EMI		
EMI1_DQ7	AT10	EMI1_DQ7	DIO			DDRIO	AVDDQ_EMI		
EMI1_DQ8	AR4	EMI1_DQ8	DIO			DDRIO	AVDDQ_EMI		
EMI1_DQ9	AU4	EMI1_DQ9	DIO			DDRIO	AVDDQ_EMI		
EMI1_DQS0_C	AM11	EMI1_DQS0_C	DIO			DDRIO	AVDDQ_EMI		
EMI1_DQS0_T	AN11	EMI1_DQS0_T	DIO			DDRIO	AVDDQ_EMI		
EMI1_DQS1_C	AT5	EMI1_DQS1_C	DIO			DDRIO	AVDDQ_EMI		
EMI1_DQS1_T	AU5	EMI1_DQS1_T	DIO			DDRIO	AVDDQ_EMI		

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EMI2_CA0	B16	EMI2_CA0	DO			DDRIO	AVDDQ_EMI		
EMI2_CA1	C16	EMI2_CA1	DO			DDRIO	AVDDQ_EMI		
EMI2_CA2	F15	EMI2_CA2	DO			DDRIO	AVDDQ_EMI		
EMI2_CA3	F16	EMI2_CA3	DO			DDRIO	AVDDQ_EMI		
EMI2_CA4	E17	EMI2_CA4	DO			DDRIO	AVDDQ_EMI		
EMI2_CA5	D17	EMI2_CA5	DO			DDRIO	AVDDQ_EMI		
EMI2_CK_C	G18	EMI2_CK_C	DO			DDRIO	AVDDQ_EMI		
EMI2_CK_T	F18	EMI2_CK_T	DO			DDRIO	AVDDQ_EMI		
EMI2_CKE0	A18	EMI2_CKE0	DO			DDRIO	AVDDQ_EMI		
EMI2_CKE1	B18	EMI2_CKE1	DO			DDRIO	AVDDQ_EMI		
EMI2_CS0	C18	EMI2_CS0	DO			DDRIO	AVDDQ_EMI		
EMI2_CS1	A16	EMI2_CS1	DO			DDRIO	AVDDQ_EMI		
EMI2_DMI0	A13	EMI2_DMI0	DIO			DDRIO	AVDDQ_EMI		
EMI2_DMI1	A7	EMI2_DMI1	DIO			DDRIO	AVDDQ_EMI		
EMI2_DQ0	A11	EMI2_DQ0	DIO			DDRIO	AVDDQ_EMI		
EMI2_DQ1	B12	EMI2_DQ1	DIO			DDRIO	AVDDQ_EMI		
EMI2_DQ10	D8	EMI2_DQ10	DIO			DDRIO	AVDDQ_EMI		
EMI2_DQ11	E9	EMI2_DQ11	DIO			DDRIO	AVDDQ_EMI		
EMI2_DQ12	C9	EMI2_DQ12	DIO			DDRIO	AVDDQ_EMI		
EMI2_DQ13	D7	EMI2_DQ13	DIO			DDRIO	AVDDQ_EMI		
EMI2_DQ14	B8	EMI2_DQ14	DIO			DDRIO	AVDDQ_EMI		
EMI2_DQ15	A9	EMI2_DQ15	DIO			DDRIO	AVDDQ_EMI		
EMI2_DQ2	G13	EMI2_DQ2	DIO			DDRIO	AVDDQ_EMI		
EMI2_DQ3	D13	EMI2_DQ3	DIO			DDRIO	AVDDQ_EMI		
EMI2_DQ4	G14	EMI2_DQ4	DIO			DDRIO	AVDDQ_EMI		
EMI2_DQ5	E13	EMI2_DQ5	DIO			DDRIO	AVDDQ_EMI		
EMI2_DQ6	B14	EMI2_DQ6	DIO			DDRIO	AVDDQ_EMI		

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Ball name	Ball location	Signal name	Signal type	Aux. function	Reset function	Buffer type	Power domain	PU/PD reset	IO reset
EMI2_DQ7	B10	EMI2_DQ7	DIO			DDRIO	AVDDQ_EMI		
EMI2_DQ8	A4	EMI2_DQ8	DIO			DDRIO	AVDDQ_EMI		
EMI2_DQ9	E7	EMI2_DQ9	DIO			DDRIO	AVDDQ_EMI		
EMI2_DQS0_C	E11	EMI2_DQS0_C	DIO			DDRIO	AVDDQ_EMI		
EMI2_DQS0_T	F11	EMI2_DQS0_T	DIO			DDRIO	AVDDQ_EMI		
EMI2_DQS1_C	C6	EMI2_DQS1_C	DIO			DDRIO	AVDDQ_EMI		
EMI2_DQS1_T	B6	EMI2_DQS1_T	DIO			DDRIO	AVDDQ_EMI		
EMI2_EXTR	B2	EMI2_EXTR	AIO			DDRIO	AVDDQ_EMI		
EMI2_RESET_N	B36	EMI2_RESET_N	DO			DDRIO	AVDDQ_EMI		
EMI2_TP	A3	EMI2_TP	AIO			DDRIO	AVDDQ_EMI		
EMI3_CA0	B22	EMI3_CA0	DO			DDRIO	AVDDQ_EMI		
EMI3_CA1	C22	EMI3_CA1	DO			DDRIO	AVDDQ_EMI		
EMI3_CA2	G23	EMI3_CA2	DO			DDRIO	AVDDQ_EMI		
EMI3_CA3	D22	EMI3_CA3	DO			DDRIO	AVDDQ_EMI		
EMI3_CA4	E22	EMI3_CA4	DO			DDRIO	AVDDQ_EMI		
EMI3_CA5	G22	EMI3_CA5	DO			DDRIO	AVDDQ_EMI		
EMI3_CK_C	G20	EMI3_CK_C	DO			DDRIO	AVDDQ_EMI		
EMI3_CK_T	F20	EMI3_CK_T	DO			DDRIO	AVDDQ_EMI		
EMI3_CKE0	A20	EMI3_CKE0	DO			DDRIO	AVDDQ_EMI		
EMI3_CKE1	B20	EMI3_CKE1	DO			DDRIO	AVDDQ_EMI		
EMI3_CS0	C20	EMI3_CS0	DO			DDRIO	AVDDQ_EMI		
EMI3_CS1	A22	EMI3_CS1	DO			DDRIO	AVDDQ_EMI		
EMI3_DMI0	A25	EMI3_DMI0	DIO			DDRIO	AVDDQ_EMI		
EMI3_DMI1	A31	EMI3_DMI1	DIO			DDRIO	AVDDQ_EMI		
EMI3_DQ0	A27	EMI3_DQ0	DIO			DDRIO	AVDDQ_EMI		
EMI3_DQ1	B26	EMI3_DQ1	DIO			DDRIO	AVDDQ_EMI		
EMI3_DQ10	E30	EMI3_DQ10	DIO			DDRIO	AVDDQ_EMI		

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Ball name	Ball location	Signal name	Signal type	Aux. function	Reset function	Buffer type	Power domain	PU/PD reset	IO reset
EMI3_DQ11	C29	EMI3_DQ11	DIO			DDRIO	AVDDQ_EMI		
EMI3_DQ12	E29	EMI3_DQ12	DIO			DDRIO	AVDDQ_EMI		
EMI3_DQ13	C32	EMI3_DQ13	DIO			DDRIO	AVDDQ_EMI		
EMI3_DQ14	B30	EMI3_DQ14	DIO			DDRIO	AVDDQ_EMI		
EMI3_DQ15	A29	EMI3_DQ15	DIO			DDRIO	AVDDQ_EMI		
EMI3_DQ2	C27	EMI3_DQ2	DIO			DDRIO	AVDDQ_EMI		
EMI3_DQ3	E25	EMI3_DQ3	DIO			DDRIO	AVDDQ_EMI		
EMI3_DQ4	G25	EMI3_DQ4	DIO			DDRIO	AVDDQ_EMI		
EMI3_DQ5	D25	EMI3_DQ5	DIO			DDRIO	AVDDQ_EMI		
EMI3_DQ6	B24	EMI3_DQ6	DIO			DDRIO	AVDDQ_EMI		
EMI3_DQ7	B28	EMI3_DQ7	DIO			DDRIO	AVDDQ_EMI		
EMI3_DQ8	C34	EMI3_DQ8	DIO			DDRIO	AVDDQ_EMI		
EMI3_DQ9	A34	EMI3_DQ9	DIO			DDRIO	AVDDQ_EMI		
EMI3_DQS0_C	F27	EMI3_DQS0_C	DIO			DDRIO	AVDDQ_EMI		
EMI3_DQS0_T	E27	EMI3_DQS0_T	DIO			DDRIO	AVDDQ_EMI		
EMI3_DQS1_C	B33	EMI3_DQS1_C	DIO			DDRIO	AVDDQ_EMI		
EMI3_DQS1_T	A33	EMI3_DQS1_T	DIO			DDRIO	AVDDQ_EMI		
DSI0_CKN_T1C	AH7	DSI0_CKN_T1C	AIO				AVDD12_DSI		
DSI0_CKP_T1B	AH6	DSI0_CKP_T1B	AIO				AVDD12_DSI		
DSI0_D0N_T1A	AH5	DSI0_D0N_T1A	AIO				AVDD12_DSI		
DSI0_D0P_T0C	AG5	DSI0_D0P_T0C	AIO				AVDD12_DSI		
DSI0_D1N_T2B	AH3	DSI0_D1N_T2B	AIO				AVDD12_DSI		
DSI0_D1P_T2A	AH4	DSI0_D1P_T2A	AIO				AVDD12_DSI		
DSI0_D2N_T0B	AG6	DSI0_D2N_T0B	AIO				AVDD12_DSI		
DSI0_D2P_T0A	AG7	DSI0_D2P_T0A	AIO				AVDD12_DSI		
DSI0_D3N	AH2	DSI0_D3N	AIO				AVDD12_DSI		
DSI0_D3P_T2C	AJ3	DSI0_D3P_T2C	AIO				AVDD12_DSI		

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Ball name	Ball location	Signal name	Signal type	Aux. function	Reset function	Buffer type	Power domain	PU/PD reset	IO reset
DSI1_CKN_T1C	AK6	DSI1_CKN_T1C	AIO				AVDD12_DSI		
DSI1_CKP_T1B	AK7	DSI1_CKP_T1B	AIO				AVDD12_DSI		
DSI1_D0N_T1A	AK5	DSI1_D0N_T1A	AIO				AVDD12_DSI		
DSI1_D0P_T0C	AL5	DSI1_D0P_T0C	AIO				AVDD12_DSI		
DSI1_D1N_T2B	AL6	DSI1_D1N_T2B	AIO				AVDD12_DSI		
DSI1_D1P_T2A	AL7	DSI1_D1P_T2A	AIO				AVDD12_DSI		
DSI1_D2N_T0B	AL4	DSI1_D2N_T0B	AIO				AVDD12_DSI		
DSI1_D2P_T0A	AL3	DSI1_D2P_T0A	AIO				AVDD12_DSI		
DSI1_D3N	AK8	DSI1_D3N	AIO				AVDD12_DSI		
DSI1_D3P_T2C	AL8	DSI1_D3P_T2C	AIO				AVDD12_DSI		
CSI0A_L0N_T0B	N3	CSI0A_L0N_T0B	AIO				AVDD12_CSI		
CSI0A_L0P_T0A	N2	CSI0A_L0P_T0A	AIO				AVDD12_CSI		
CSI0A_L1N_T1A	N5	CSI0A_L1N_T1A	AIO				AVDD12_CSI		
CSI0A_L1P_T0C	N4	CSI0A_L1P_T0C	AIO				AVDD12_CSI		
CSI0A_L2N_T1C	N6	CSI0A_L2N_T1C	AIO				AVDD12_CSI		
CSI0A_L2P_T1B	M6	CSI0A_L2P_T1B	AIO				AVDD12_CSI		
CSI0B_L0N_T0B	P1	CSI0B_L0N_T0B	AIO				AVDD12_CSI		
CSI0B_L0P_T0A	P2	CSI0B_L0P_T0A	AIO				AVDD12_CSI		
CSI0B_L1N_T1A	P4	CSI0B_L1N_T1A	AIO				AVDD12_CSI		
CSI0B_L1P_T0C	P3	CSI0B_L1P_T0C	AIO				AVDD12_CSI		
CSI0B_L2N_T1C	P6	CSI0B_L2N_T1C	AIO				AVDD12_CSI		
CSI0B_L2P_T1B	P5	CSI0B_L2P_T1B	AIO				AVDD12_CSI		
CSI1A_L0N_T0B	J4	CSI1A_L0N_T0B	AIO				AVDD12_CSI		
CSI1A_L0P_T0A	J5	CSI1A_L0P_T0A	AIO				AVDD12_CSI		
CSI1A_L1N_T1A	J3	CSI1A_L1N_T1A	AIO				AVDD12_CSI		
CSI1A_L1P_T0C	J2	CSI1A_L1P_T0C	AIO				AVDD12_CSI		
CSI1A_L2N_T1C	K6	CSI1A_L2N_T1C	AIO				AVDD12_CSI		

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Ball name	Ball location	Signal name	Signal type	Aux. function	Reset function	Buffer type	Power domain	PU/PD reset	IO reset
CSI1A_L2P_T1B	K7	CSI1A_L2P_T1B	AIO				AVDD12_CSI		
CSI1B_L0N_T0B	K3	CSI1B_L0N_T0B	AIO				AVDD12_CSI		
CSI1B_L0P_T0A	K5	CSI1B_L0P_T0A	AIO				AVDD12_CSI		
CSI1B_L1N_T1A	L4	CSI1B_L1N_T1A	AIO				AVDD12_CSI		
CSI1B_L1P_T0C	L3	CSI1B_L1P_T0C	AIO				AVDD12_CSI		
SSUSB_RXN	W36	SSUSB_RXN	AI				AVDD12_SSUSB		
SSUSB_RXP	W37	SSUSB_RXP	AI				AVDD12_SSUSB		
SSUSB_TXN	Y34	SSUSB_TXN	AO				AVDD12_SSUSB		
SSUSB_TXP	Y33	SSUSB_TXP	AO				AVDD12_SSUSB		
PCIE_CKN	AN3	PCIE_CKN	AIO				AVDD12_PCIE		
PCIE_CKP	AN4	PCIE_CKP	AIO				AVDD12_PCIE		
PCIE_LN0_RXN	AP1	PCIE_LN0_RXN	AIO				AVDD12_PCIE		
PCIE_LN0_RXP	AP2	PCIE_LN0_RXP	AIO				AVDD12_PCIE		
PCIE_LN0_TXN	AM2	PCIE_LN0_TXN	AIO				AVDD12_PCIE		
PCIE_LN0_TXP	AM1	PCIE_LN0_TXP	AIO				AVDD12_PCIE		
DP_LN0_TXN	AH35	DP_LN0_TXN	AIO				AVDD12_DPTX		
DP_LN0_TXP	AG35	DP_LN0_TXP	AIO				AVDD12_DPTX		
DP_LN1_TXN	AH31	DP_LN1_TXN	AIO				AVDD12_DPTX		
DP_LN1_TXP	AH32	DP_LN1_TXP	AIO				AVDD12_DPTX		
DP_LN2_TXN	AJ33	DP_LN2_TXN	AIO				AVDD12_DPTX		
DP_LN2_TXP	AJ34	DP_LN2_TXP	AIO				AVDD12_DPTX		
DP_LN3_TXN	AK31	DP_LN3_TXN	AIO				AVDD12_DPTX		
DP_LN3_TXP	AK32	DP_LN3_TXP	AIO				AVDD12_DPTX		
DPAUXN	AJ37	DPAUXN	AIO				AVDD12_DPTX		
DPAUXP	AJ36	DPAUXP	AIO				AVDD12_DPTX		
EDP_LN0_TXN	AG29	EDP_LN0_TXN	AIO				AVDD12_EDPTX		
EDP_LN0_TXP	AG30	EDP_LN0_TXP	AIO				AVDD12_EDPTX		

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Ball name	Ball location	Signal name	Signal type	Aux. function	Reset function	Buffer type	Power domain	PU/PD reset	IO reset
EDP_LN1_TXN	AF31	EDP_LN1_TXN	AIO				AVDD12_EDPTX		
EDP_LN1_TXP	AF32	EDP_LN1_TXP	AIO				AVDD12_EDPTX		
EDPAUXN	AF37	EDPAUXN	AIO				AVDD12_EDPTX		
EDPAUXP	AF36	EDPAUXP	AIO				AVDD12_EDPTX		
USB_DM_P0	W31	USB_DM_P0	AIO				AVDD33_USB_P0		
USB_DM_P1	U36	USB_DM_P1	AIO				AVDD33_USB_P1		
USB_DM_P2	V35	USB_DM_P2	AIO				AVDD33_USB_P2		
USB_DP_P0	W32	USB_DP_P0	AIO				AVDD33_USB_P0		
USB_DP_P1	U37	USB_DP_P1	AIO				AVDD33_USB_P1		
USB_DP_P2	V34	USB_DP_P2	AIO				AVDD33_USB_P2		
AUXIN0	AE6	AUXIN0	AIO				AVDD18_AUXADC		
AUXIN1	AF2	AUXIN1	AIO				AVDD18_AUXADC		
AUXIN2	AE3	AUXIN2	AIO				AVDD18_AUXADC		
AUXIN3	AE2	AUXIN3	AIO				AVDD18_AUXADC		
AUXIN4	AE4	AUXIN4	AIO				AVDD18_AUXADC		
AUXIN5	AE5	AUXIN5	AIO				AVDD18_AUXADC		
REFP	AE7	REFP	AIO				AVDD18_AUXADC		
HDMITX21_CH0_M	AN34	HDMITX21_CH0_M	AIO				AVDD18_HDMITX21		
HDMITX21_CH0_P	AN35	HDMITX21_CH0_P	AIO				AVDD18_HDMITX21		
HDMITX21_CH1_M	AM37	HDMITX21_CH1_M	AIO				AVDD18_HDMITX21		
HDMITX21_CH1_P	AM36	HDMITX21_CH1_P	AIO				AVDD18_HDMITX21		
HDMITX21_CH2_M	AL35	HDMITX21_CH2_M	AIO				AVDD18_HDMITX21		
HDMITX21_CH2_P	AK35	HDMITX21_CH2_P	AIO				AVDD18_HDMITX21		
HDMITX21_CLK_M	AR35	HDMITX21_CLK_M	AIO				AVDD18_HDMITX21		
HDMITX21_CLK_P	AR34	HDMITX21_CLK_P	AIO				AVDD18_HDMITX21		
DDR4									
EMI0_ACT_N	AT18	EMI0_ACT_N	DO				AVDDQ_EMI		

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Ball name	Ball location	Signal name	Signal type	Aux. function	Reset function	Buffer type	Power domain	PU/PD reset	IO reset
EMI0_BA0	AL16	EMI0_BA0	DO				AVDDQ_EMI		
EMI0_BA1	AN21	EMI0_BA1	DO				AVDDQ_EMI		
EMI0_BG0	AT16	EMI0_BG0	DO				AVDDQ_EMI		
EMI0_CA0	AN16	EMI0_CA0	DO				AVDDQ_EMI		
EMI0_CA1	AP21	EMI0_CA1	DO				AVDDQ_EMI		
EMI0_CA10	AR16	EMI0_CA10	DO				AVDDQ_EMI		
EMI0_CA11	AK19	EMI0_CA11	DO				AVDDQ_EMI		
EMI0_CA12	AT22	EMI0_CA12	DO				AVDDQ_EMI		
EMI0_CA13	AM18	EMI0_CA13	DO				AVDDQ_EMI		
EMI0_CA2	AL18	EMI0_CA2	DO				AVDDQ_EMI		
EMI0_CA3	AU22	EMI0_CA3	DO				AVDDQ_EMI		
EMI0_CA4	AU16	EMI0_CA4	DO				AVDDQ_EMI		
EMI0_CA5	AM22	EMI0_CA5	DO				AVDDQ_EMI		
EMI0_CA6	AP16	EMI0_CA6	DO				AVDDQ_EMI		
EMI0_CA7	AM23	EMI0_CA7	DO				AVDDQ_EMI		
EMI0_CA8	AL15	EMI0_CA8	DO				AVDDQ_EMI		
EMI0_CA9	AL22	EMI0_CA9	DO				AVDDQ_EMI		
EMI0_CAS_N	AM15	EMI0_CAS_N	DO				AVDDQ_EMI		
EMI0_CK_C	AL20	EMI0_CK_C	DO				AVDDQ_EMI		
EMI0_CK_T	AM20	EMI0_CK_T	DO				AVDDQ_EMI		
EMI0_CKE0	AU20	EMI0_CKE0	DO				AVDDQ_EMI		
EMI0_CS0	AR20	EMI0_CS0	DO				AVDDQ_EMI		
EMI0_DMI0	AU31	EMI0_DMI0	DIO				AVDDQ_EMI		
EMI0_DMI1	AU25	EMI0_DMI1	DIO				AVDDQ_EMI		
EMI0_DQ0	AN25	EMI0_DQ0	DIO				AVDDQ_EMI		
EMI0_DQ1	AT28	EMI0_DQ1	DIO				AVDDQ_EMI		
EMI0_DQ10	AU27	EMI0_DQ10	DIO				AVDDQ_EMI		

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Ball name	Ball location	Signal name	Signal type	Aux. function	Reset function	Buffer type	Power domain	PU/PD reset	IO reset
EMI0_DQ11	AT30	EMI0_DQ11	DIO				AVDDQ_EMI		
EMI0_DQ12	AT24	EMI0_DQ12	DIO				AVDDQ_EMI		
EMI0_DQ13	AN31	EMI0_DQ13	DIO				AVDDQ_EMI		
EMI0_DQ14	AL25	EMI0_DQ14	DIO				AVDDQ_EMI		
EMI0_DQ15	AU29	EMI0_DQ15	DIO				AVDDQ_EMI		
EMI0_DQ2	AP25	EMI0_DQ2	DIO				AVDDQ_EMI		
EMI0_DQ3	AP30	EMI0_DQ3	DIO				AVDDQ_EMI		
EMI0_DQ4	AL24	EMI0_DQ4	DIO				AVDDQ_EMI		
EMI0_DQ5	AP31	EMI0_DQ5	DIO				AVDDQ_EMI		
EMI0_DQ6	AN29	EMI0_DQ6	DIO				AVDDQ_EMI		
EMI0_DQ7	AR29	EMI0_DQ7	DIO				AVDDQ_EMI		
EMI0_DQ8	AT26	EMI0_DQ8	DIO				AVDDQ_EMI		
EMI0_DQ9	AU34	EMI0_DQ9	DIO				AVDDQ_EMI		
EMI0_DQS0_C	AN27	EMI0_DQS0_C	DO				AVDDQ_EMI		
EMI0_DQS0_T	AM27	EMI0_DQS0_T	DO				AVDDQ_EMI		
EMI0_DQS1_C	AR32	EMI0_DQS1_C	DO				AVDDQ_EMI		
EMI0_DQS1_T	AT32	EMI0_DQS1_T	DO				AVDDQ_EMI		
EMI0_EXTR	AT2	EMI0_EXTR	AIO				AVDDQ_EMI		
EMI0_ODT	AP19	EMI0_ODT	AIO				AVDDQ_EMI		
EMI0_RAS_N	AR22	EMI0_RAS_N	DO				AVDDQ_EMI		
EMI0_RESET_N	AU35	EMI0_RESET_N	DO				AVDDQ_EMI		
EMI0_TP	AR3	EMI0_TP	AIO				AVDDQ_EMI		
EMI0_WE_N	AT20	EMI0_WE_N	DO				AVDDQ_EMI		
EMI1_CKE0	AU18	EMI1_CKE0	DO				AVDDQ_EMI		
EMI1_CS0	AR18	EMI1_CS0	DO				AVDDQ_EMI		
EMI1_DMI0	AU13	EMI1_DMI0	DIO				AVDDQ_EMI		
EMI1_DMI1	AU7	EMI1_DMI1	DIO				AVDDQ_EMI		

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Ball name	Ball location	Signal name	Signal type	Aux. function	Reset function	Buffer type	Power domain	PU/PD reset	IO reset
EMI1_DQ0	AU4	EMI1_DQ0	DIO				AVDDQ_EMI		
EMI1_DQ1	AL13	EMI1_DQ1	DIO				AVDDQ_EMI		
EMI1_DQ10	AT10	EMI1_DQ10	DIO				AVDDQ_EMI		
EMI1_DQ11	AT12	EMI1_DQ11	DIO				AVDDQ_EMI		
EMI1_DQ12	AT8	EMI1_DQ12	DIO				AVDDQ_EMI		
EMI1_DQ13	AT14	EMI1_DQ13	DIO				AVDDQ_EMI		
EMI1_DQ14	AR4	EMI1_DQ14	DIO				AVDDQ_EMI		
EMI1_DQ15	AU11	EMI1_DQ15	DIO				AVDDQ_EMI		
EMI1_DQ2	AN8	EMI1_DQ2	DIO				AVDDQ_EMI		
EMI1_DQ3	AN13	EMI1_DQ3	DIO				AVDDQ_EMI		
EMI1_DQ4	AR6	EMI1_DQ4	DIO				AVDDQ_EMI		
EMI1_DQ5	AP13	EMI1_DQ5	DIO				AVDDQ_EMI		
EMI1_DQ6	AN9	EMI1_DQ6	DIO				AVDDQ_EMI		
EMI1_DQ7	AR9	EMI1_DQ7	DIO				AVDDQ_EMI		
EMI1_DQ8	AU9	EMI1_DQ8	DIO				AVDDQ_EMI		
EMI1_DQ9	AR11	EMI1_DQ9	DIO				AVDDQ_EMI		
EMI1_DQS0_C	AT5	EMI1_DQS0_C	DIO				AVDDQ_EMI		
EMI1_DQS0_T	AU5	EMI1_DQS0_T	DIO				AVDDQ_EMI		
EMI1_DQS1_C	AM11	EMI1_DQS1_C	DIO				AVDDQ_EMI		
EMI1_DQS1_T	AN11	EMI1_DQS1_T	DIO				AVDDQ_EMI		
EMI2_ACT_N	B20	EMI2_ACT_N	DO				AVDDQ_EMI		
EMI2_BA0	G22	EMI2_BA0	DO				AVDDQ_EMI		
EMI2_BA1	E17	EMI2_BA1	DO				AVDDQ_EMI		
EMI2_BG0	B22	EMI2_BG0	DO				AVDDQ_EMI		
EMI2_CA0	E22	EMI2_CA0	DO				AVDDQ_EMI		
EMI2_CA1	D17	EMI2_CA1	DO				AVDDQ_EMI		
EMI2_CA10	C22	EMI2_CA10	DO				AVDDQ_EMI		

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Ball name	Ball location	Signal name	Signal type	Aux. function	Reset function	Buffer type	Power domain	PU/PD reset	IO reset
EMI2_CA11	H19	EMI2_CA11	DO				AVDDQ_EMI		
EMI2_CA12	B16	EMI2_CA12	DO				AVDDQ_EMI		
EMI2_CA13	F20	EMI2_CA13	DO				AVDDQ_EMI		
EMI2_CA2	G20	EMI2_CA2	DO				AVDDQ_EMI		
EMI2_CA3	A16	EMI2_CA3	DO				AVDDQ_EMI		
EMI2_CA4	A22	EMI2_CA4	DO				AVDDQ_EMI		
EMI2_CA5	F16	EMI2_CA5	DO				AVDDQ_EMI		
EMI2_CA6	D22	EMI2_CA6	DO				AVDDQ_EMI		
EMI2_CA7	F15	EMI2_CA7	DO				AVDDQ_EMI		
EMI2_CA8	G23	EMI2_CA8	DO				AVDDQ_EMI		
EMI2_CA9	G16	EMI2_CA9	DO				AVDDQ_EMI		
EMI2_CAS_N	F23	EMI2_CAS_N	DO				AVDDQ_EMI		
EMI2_CK_C	G18	EMI2_CK_C	DO				AVDDQ_EMI		
EMI2_CK_T	F18	EMI2_CK_T	DO				AVDDQ_EMI		
EMI2_CKE0	A18	EMI2_CKE0	DO				AVDDQ_EMI		
EMI2_CS0	C18	EMI2_CS0	DO				AVDDQ_EMI		
EMI2_DMI0	A7	EMI2_DMI0	DIO				AVDDQ_EMI		
EMI2_DMI1	A13	EMI2_DMI1	DIO				AVDDQ_EMI		
EMI2_DQ0	E13	EMI2_DQ0	DIO				AVDDQ_EMI		
EMI2_DQ1	B10	EMI2_DQ1	DIO				AVDDQ_EMI		
EMI2_DQ10	A11	EMI2_DQ10	DIO				AVDDQ_EMI		
EMI2_DQ11	B8	EMI2_DQ11	DIO				AVDDQ_EMI		
EMI2_DQ12	B14	EMI2_DQ12	DIO				AVDDQ_EMI		
EMI2_DQ13	E7	EMI2_DQ13	DIO				AVDDQ_EMI		
EMI2_DQ14	G13	EMI2_DQ14	DIO				AVDDQ_EMI		
EMI2_DQ15	A9	EMI2_DQ15	DIO				AVDDQ_EMI		
EMI2_DQ2	D13	EMI2_DQ2	DIO				AVDDQ_EMI		

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Ball name	Ball location	Signal name	Signal type	Aux. function	Reset function	Buffer type	Power domain	PU/PD reset	IO reset
EMI2_DQ3	D8	EMI2_DQ3	DIO				AVDDQ_EMI		
EMI2_DQ4	G14	EMI2_DQ4	DIO				AVDDQ_EMI		
EMI2_DQ5	D7	EMI2_DQ5	DIO				AVDDQ_EMI		
EMI2_DQ6	E9	EMI2_DQ6	DIO				AVDDQ_EMI		
EMI2_DQ7	C9	EMI2_DQ7	DIO				AVDDQ_EMI		
EMI2_DQ8	B12	EMI2_DQ8	DIO				AVDDQ_EMI		
EMI2_DQ9	A4	EMI2_DQ9	DIO				AVDDQ_EMI		
EMI2_DQS0_C	E11	EMI2_DQS0_C	DIO				AVDDQ_EMI		
EMI2_DQS0_T	F11	EMI2_DQS0_T	DIO				AVDDQ_EMI		
EMI2_DQS1_C	C6	EMI2_DQS1_C	DIO				AVDDQ_EMI		
EMI2_DQS1_T	B6	EMI2_DQS1_T	DIO				AVDDQ_EMI		
EMI2_EXTR	B2	EMI2_EXTR	AIO				AVDDQ_EMI		
EMI2_ODT	D19	EMI2_ODT	AIO				AVDDQ_EMI		
EMI2_RAS_N	C16	EMI2_RAS_N	DO				AVDDQ_EMI		
EMI2_RESET_N	B36	EMI2_RESET_N	DO				AVDDQ_EMI		
EMI2_TP	A3	EMI2_TP	AIO				AVDDQ_EMI		
EMI2_WE_N	B18	EMI2_WE_N	DO				AVDDQ_EMI		
EMI3_CKE0	A20	EMI3_CKE0	DO				AVDDQ_EMI		
EMI3_CS0	C20	EMI3_CS0	DO				AVDDQ_EMI		
EMI3_DMI0	A25	EMI3_DMI0	DIO				AVDDQ_EMI		
EMI3_DMI1	A31	EMI3_DMI1	DIO				AVDDQ_EMI		
EMI3_DQ0	A34	EMI3_DQ0	DIO				AVDDQ_EMI		
EMI3_DQ1	G25	EMI3_DQ1	DIO				AVDDQ_EMI		
EMI3_DQ10	B28	EMI3_DQ10	DIO				AVDDQ_EMI		
EMI3_DQ11	B26	EMI3_DQ11	DIO				AVDDQ_EMI		
EMI3_DQ12	B30	EMI3_DQ12	DIO				AVDDQ_EMI		
EMI3_DQ13	B24	EMI3_DQ13	DIO				AVDDQ_EMI		

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Ball name	Ball location	Signal name	Signal type	Aux. function	Reset function	Buffer type	Power domain	PU/PD reset	IO reset
EMI3_DQ14	C34	EMI3_DQ14	DIO				AVDDQ_EMI		
EMI3_DQ15	A27	EMI3_DQ15	DIO				AVDDQ_EMI		
EMI3_DQ2	E30	EMI3_DQ2	DIO				AVDDQ_EMI		
EMI3_DQ3	E25	EMI3_DQ3	DIO				AVDDQ_EMI		
EMI3_DQ4	C32	EMI3_DQ4	DIO				AVDDQ_EMI		
EMI3_DQ5	D25	EMI3_DQ5	DIO				AVDDQ_EMI		
EMI3_DQ6	E29	EMI3_DQ6	DIO				AVDDQ_EMI		
EMI3_DQ7	C29	EMI3_DQ7	DIO				AVDDQ_EMI		
EMI3_DQ8	A29	EMI3_DQ8	DIO				AVDDQ_EMI		
EMI3_DQ9	C27	EMI3_DQ9	DIO				AVDDQ_EMI		
EMI3_DQS0_C	B33	EMI3_DQS0_C	DIO				AVDDQ_EMI		
EMI3_DQS0_T	A33	EMI3_DQS0_T	DIO				AVDDQ_EMI		
EMI3_DQS1_C	F27	EMI3_DQS1_C	DIO				AVDDQ_EMI		
EMI3_DQS1_T	E27	EMI3_DQS1_T	DIO				AVDDQ_EMI		

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4.3 Power Rails

Table 4-20 Power rails

Ball name	Ball location	Type	Description
AVDD2_EMI0	AH15, AH17, AH19, AH21, AH23	P	DRAM power
AVDD2_EMI2	K15, K17, K19, K21, K23	P	DRAM power
AVDD12_AUXADC	AE1	P	Analog power for AUXADC
AVDD12_CKSQ	AD28	P	Analog power for CKSQ
AVDD12_CSI0	P8	P	Analog power for CSI0
AVDD12_CSI1	M9	P	Analog power for CSI1
AVDD12_DPTX	AJ29	P	Analog power for DPTX
AVDD12_DSI	AH10	P	Analog power for DSI
AVDD12_EDPTX	AG27	P	Analog power for EDPTX
AVDD12_EMI0	AJ14	P	DRAM power
AVDD12_EMI2	J13	P	DRAM power
AVDD12_HDMITX21	AL28	P	Analog power for HDMITX
AVDD12_PCIE	AJ11	P	Analog power for PCIE
AVDD12_PLLGP1	U19	P	Analog power for APPLL
AVDD12_PLLGP2	AC16	P	Analog power for APPLL
AVDD12_PLLGP34	V14, W14	P	Analog power for APPLL
AVDD12_SSUSB	AC28	P	Analog power for SSUSB
AVDD12_USB_P0	W29	P	Analog power for USB_P0
AVDD12_USB_P1	Y28	P	Analog power for USB_P1
AVDD12_USB_P2	Y29	P	Analog power for USB_P2
AVDD18_APU	W17	P	Analog power 1.8V for APU
AVDD18_AUXADC	AF1	P	Analog power 1.8V for AUXADC
AVDD18_CKSQ	AD29	P	Analog power 1.8V for CKSQ
AVDD18_DPTX	AH28	P	Analog power 1.8V for DPTX
AVDD18_DSI	AE10	P	Analog power 1.8V for DSI
AVDD18_EDPTX	AG26	P	Analog power 1.8V for EDPTX
AVDD18_EMI0	AH25	P	DRAM power
AVDD18_EMI2	J24	P	DRAM power
AVDD18_HDMITX21	AL29	P	Analog power 1.8V for HDMITX
AVDD18_PCIE	AH11	P	Analog power 1.8V for PCIE
AVDD18_PLLGP1	V20	P	Analog power 1.8V for APPLL
AVDD18_PLLGP2	AC17	P	Analog power 1.8V for APPLL
AVDD18_PLLGP34	V13, W13	P	Analog power 1.8V for APPLL
AVDD18_PROC	L24	P	Analog power 1.8V for CPU
AVDD18_SSUSB	AC29	P	Analog power 1.8V for SSUSB
AVDD18_USB_P0	W28	P	Analog power 1.8V for USB_P0
AVDD18_USB_P1	AA29	P	Analog power 1.8V for USB_P1
AVDD18_USB_P2	U28	P	Analog power 1.8V for USB_P2
AVDD33_USB_P0	U33	P	Analog power 3.3V for USB_P0

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Ball name	Ball location	Type	Description
AVDD33_USB_P1	V32	P	Analog power 3.3V for USB_P1
AVDD33_USB_P2	U29	P	Analog power 3.3V for USB_P2
AVDD075_DRV_DSI	AE11	P	Analog power for DSI
AVDD075_EMI0	AH14, AH24	P	DRAM power
AVDD075_EMI2	K13, K24	P	DRAM power
AVDDQ_EMI0	AH16, AH18, AH20, AH22, AJ15, AJ17, AJ19, AJ21, AJ23, AJ24	P	DRAM power
AVDDQ_EMI2	J15, J17, J19, J21, J23, K14, K16, K18, K20, K22	P	DRAM power
DVDD_ADSP	AD19, AD20, AE19, AE20, AF19, AF20	P	Digital power input for ADSP
DVDD_APU	V16, W16, Y13, Y14, Y16, Y17, AA13, AA14, AA16, AA17, AB14, AB16	P	Digital power input for APU
DVDD_CORE	L13, M20, N20, P15, R15, T19, U12, U13, U14, U15, U16, U17, U20, V17, V18, W19, W20, Y19, Y20, Y23, Y24, Y25, AA19, AA20, AA23, AA24, AB19, AB20, AB23, AB24, AC19, AC20, AC23, AC24, AD23, AD24, AE23, AE24, AF23, AF24, AG14	P	Digital power input for Vcore
DVDD_GPU	AC14, AC15, AD13, AD14, AD15, AD16, AE13, AE14, AE15, AE16, AF14, AF15, AF16, AF17	P	Digital power input for GPU
DVDD_MM	M14, M18, M19, N14, N15, N17, N19, P14, P17, P19, P20, R14, R17, R19, R20, T14, T15, T16, T17	P	Digital power input for ISP
DVDD_PROC_B	K26, K27, K28, L21, L26, L27, L28, M21, M25, M26, M27, M28, N21, N22, N24, N25	P	Digital power input for Big Core
DVDD_PROC_L	P24, R22, R25, R26, R27, T22, T25, T26, T27, T28, U22, U24, U25, U26, U27, V22, V27, W24	P	Digital power input for Little Core
DVDD_SRAM_APU	AB13	P	Digital power input for APU SRAM
DVDD_SRAM_CORE	Y22, AD22, AF22	P	Digital power input for Core SRAM
DVDD_SRAM_GPU	AC13, AF13	P	Digital power input for GPU SRAM
DVDD_SRAM_MM	M16, R13	P	Digital power input for ISP SRAM
DVDD_SRAM_PROC_B	M22, N26	P	Digital power input for Big Core SRAM
DVDD_SRAM_PROC_L	R21, V24	P	Digital power input for Little Core SRAM
DVDD18_IODPI	AD1	P	Digital power input for I/O
DVDD18_IOEMMC	C37	P	Digital power input for I/O
DVDD18_IOLM	AD31	P	Digital power input for I/O
DVDD18_IOLT	G37, R37	P	Digital power input for I/O
DVDD18_IORM	AA10	P	Digital power input for I/O
DVDD18_IORT	J11	P	Digital power input for I/O
DVDD18_MSDC1	E1	P	Digital power input for I/O
DVDD18_MSDC2	AB36	P	Digital power input for I/O
DVDD18_VQPS	H27	DIO	eFuse blowing power input

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Ball name	Ball location	Type	Description
DVDD28_IODPI	U9	P	Digital power input for DPI
DVDD28_MSDC1	G7	P	Digital power input for MSDC1
DVDD28_MSDC2	AA36	P	Digital power input for MSDC2
DVSS	A5, A6, A32, A35, B3, B4, B5, B7, B9, B11, B13, B15, B23, B25, B27, B29, B31, B32, B34, B35, C2, C5, C7, C8, C10, C11, C12, C13, C14, C15, C17, C19, C21, C23, C24, C25, C26, C28, C30, C31, C33, C35, C36, D5, D6, D9, D10, D11, D12, D14, D15, D16, D18, D20, D21, D23, D24, D26, D27, D28, D29, D30, D31, D32, D34, E6, E8, E10, E12, E14, E15, E16, E18, E19, E20, E21, E23, E24, E26, E28, E31, E33, F7, F8, F9, F10, F12, F13, F14, F17, F19, F21, F22, F24, F25, F26, F28, F29, F30, F31, F34, F35, G8, G9, G10, G11, G12, G15, G17, G19, G21, G24, G26, G27, G28, G29, G34, G35, H4, H5, H6, H8, H9, H10, H11, H12, H13, H14, H15, H16, H17, H18, H20, H21, H22, H23, H24, H25, H26, H28, H29, H30, J1, J6, J7, J8, J9, J10, J12, J14, J16, J18, J20, J22, J25, J26, J27, J28, J29, K4, K8, K9, K10, K11, K25, K29, L5, L6, L7, L8, L9, L10, L11, L23, L25, L29, M4, M5, M7, M8, M10, M11, M13, M15, M17, M23, M24, M29, M37, N1, N7, N10, N13, N16, N18, N23, N27, N28, N29, N36, P7, P9, P10, P11, P13, P16, P18, P21, P22, P23, P25, P26, P27, P28, P29, R3, R4, R5, R6, R7, R8, R9, R10, R11, R16, R18, R23, R24, R28, R29, T3, T13, T18, T23, T24, T29, T35, T36, T37, U21, U23, U30, U31, U34, U35, V12, V15, V21, V23, V25, V26, V29, V30, V31, V33, V36, W12, W15, W18, W21, W22, W23, W25, W30, W33, W34, W35, Y15, Y18, Y21, Y27, Y30, Y31, Y32, Y35, Y36, AA15, AA18, AA21, AA22, AA25, AA26, AA27, AA32, AA33, AA34, AB12, AB15, AB17, AB18, AB21, AB22, AB25, AB27, AB29, AB30, AC12, AC18, AC21, AC22, AC25, AC27, AD2, AD3, AD4, AD5, AD6, AD7, AD8, AD9, AD12, AD17, AD18, AD21, AD25, AD26, AD34, AE8, AE9, AE12, AE17, AE18, AE21, AE22, AE27, AE28, AE29, AE30, AE31, AE32, AE33, AE35, AE36, AF3, AF4, AF5, AF6, AF7, AF8, AF9, AF10, AF12, AF18, AF21, AF26, AF27, AF28, AF29, AF30, AF33, AF34, AF35, AG4, AG8, AG9, AG11, AG28, AG31, AG32, AG33, AG34, AH1, AH8, AH9, AH12, AH29, AH30, AH33, AH34, AJ4, AJ5, AJ6, AJ7, AJ8, AJ9, AJ12, AJ13, AJ16, AJ18, AJ20, AJ22, AJ25, AJ26, AJ27, AJ28, AJ30, AJ31, AJ32, AJ35, AK9, AK10, AK11, AK12, AK13, AK14, AK15, AK16, AK17, AK18, AK20, AK21, AK22,	G	GND

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Ball name	Ball location	Type	Description
	AK23, AK24, AK25, AK26, AK27, AK28, AK29, AK30, AK33, AK34, AL1, AL2, AL9, AL10, AL11, AL12, AL14, AL17, AL19, AL21, AL23, AL26, AL27, AL31, AL32, AL33, AL34, AM3, AM4, AM5, AM6, AM7, AM8, AM9, AM10, AM12, AM13, AM14, AM16, AM17, AM19, AM21, AM24, AM25, AM26, AM28, AM29, AM30, AM31, AM32, AM33, AM34, AM35, AN2, AN5, AN6, AN7, AN10, AN12, AN14, AN15, AN17, AN18, AN19, AN20, AN22, AN23, AN24, AN26, AN28, AN30, AN32, AN33, AP3, AP4, AP5, AP6, AP7, AP8, AP9, AP10, AP11, AP12, AP14, AP15, AP17, AP18, AP20, AP22, AP23, AP24, AP26, AP27, AP28, AP29, AP32, AP33, AP34, AP36, AP37, AR2, AR5, AR7, AR8, AR10, AR12, AR13, AR14, AR15, AR17, AR19, AR21, AR23, AR24, AR25, AR26, AR27, AR28, AR30, AR31, AR33, AT3, AT4, AT6, AT7, AT9, AT11, AT13, AT15, AT23, AT25, AT27, AT29, AT31, AT33, AT34, AT35, AT36, AU3, AU6, AU32, AU33		

4.4 Reserved and Unused Pin Handling Recommendations

MT8390 Baseband Design Notice provides specific pin handling recommendations for the case that the pins are not used.

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5 Electrical Characteristics

Stresses above the values listed in Table 5-1 may cause permanent damage to the device. The recommended minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage, and frequencies based on characterization results. Exposure to absolute maximum rating conditions may affect device reliability. The operating conditions in Table 5-2 must not be exceeded in order to ensure correct operation and reliability of the device. All parameters specified in this document refer to these operating conditions, unless noted otherwise.

5.1 Absolute Maximum Ratings

Table 5-1 Absolute maximum ratings

Parameter	Conditions	Max.	Unit
Digital power input for A78 core	DVDD_PROC_B, DVDD_SRAM_PROC_B	1.21	V
Digital power input for A55 core	DVDD_PROC_L	0.99	V
Digital power input for A55 core	DVDD_SRAM_PROC_L	1.08	V
Digital power input for Vcore	DVDD_CORE	0.83	V
Digital power input for GPU	DVDD_GPU	0.88	V
Analog power input	AVDD12_AUXADC, AVDD12_CKSQ, AVDD12_CSI0, AVDD12_CSI1, AVDD12_DPTX, AVDD12_DSI, AVDD12_EDPTX, AVDD12_HDMITX21, AVDD12_PCIE, AVDD12_PLLGP1, AVDD12_PLLGP2, AVDD12_PLLGP34, AVDD12_SSUSB, AVDD12_USB_P0, AVDD12_USB_P1, AVDD12_USB_P2, AVDD12_EMI0, AVDD12_EMI2, AVDD2_EMI0, AVDD2_EMI2, AVDDQ_EMI0, AVDDQ_EMI2	1.32	V
	AVDD18_APU, AVDD18_AUXADC, AVDD18_CKSQ, AVDD18_DPTX, AVDD18_DSI, AVDD18_EDPTX, AVDD18_HDMITX21, AVDD18_PCIE, AVDD18_PLLGP1, AVDD18_PLLGP2, AVDD18_PLLGP34, AVDD18_PROC, AVDD18_SSUSB, AVDD18_USB_P0, AVDD18_USB_P1, AVDD18_USB_P2, AVDD18_EMI0, AVDD18_EMI2	1.98	V
	AVDD33_USB_P0, AVDD33_USB_P1, AVDD33_USB_P2	3.22	V
	AVDD075_EMI0, AVDD075_EMI2	0.825	V
Digital power input	DVDD_ADSP, DVDD_MM, DVDD_SRAM_CORE, DVDD_SRAM_MM	0.83	V
	DVDD_APU	0.85	V

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Parameter	Conditions	Max.	Unit
	DVDD_SRAM_APU	0.88	V
	DVDD_SRAM_GPU	0.94	V
	DVDD18_IODPI, DVDD18_IOEMMC, DVDD18_IOLM, DVDD18_IOLT, DVDD18_IORM, DVDD18_IORT, DVDD18_MSDC1, DVDD18_MSDC2	1.95	V
	DVDD28_IODPI, DVDD28_MSDC1 DVDD28_MSDC2	3.15	V

Warning: Stressing the device beyond the absolute maximum ratings may cause permanent damage. These are stress ratings only.

5.1.1 Storage Condition

Table 5-2 defines storage conditions specifics.

Table 5-2 Storage condition

Parameter		Min.	Max.	Unit
Shelf life in sealed bag	40°C/90% RH		24	Months
After bag opened(1)				
Mounted	30°C/60% RH		168	h
Stored			20	% RH
Baking				
Low temperature device containers	40°C +5°C/-0°C and < 5% RH	192		h
High temperature device containers	125°C +5°C/-0°C	24		h

1. For devices subjected to infrared reflow, vapor-phase reflow, or equivalent processing.

5.2 Recommended Operating Conditions

Table 5-3 presents the recommended operating conditions of the device power pins.

Table 5-3 Recommended operating conditions for power supply

Pin name	Description	Min.	Typ.	Max.	Unit
AVDD075_DRV_DSI	Analog power for DRV_DSI	0.7125	0.75	0.7875	V
AVDD12_AUXADC	Analog power for AUXADC	1.14	1.2	1.26	V
AVDD12_CKSQ	Analog power for CKSQ	1.14	1.2	1.26	V
AVDD12_CSI0	Analog power for CSI0	1.14	1.2	1.26	V
AVDD12_CSI1	Analog power for CSI1	1.14	1.2	1.26	V
AVDD12_DPTX	Analog power for DPTX	1.14	1.2	1.26	V
AVDD12_DSI	Analog power for DSI	1.14	1.2	1.26	V
AVDD12_EDPTX	Analog power for EDPTX	1.14	1.2	1.26	V
AVDD12_HDMITX21	Analog power for HDMITX21	1.14	1.2	1.26	V
AVDD12_PCIE	Analog power for PCIe	1.14	1.2	1.26	V
AVDD12_PLLGP1	Analog power for PLLGP1	1.14	1.2	1.26	V
AVDD12_PLLGP2	Analog power for PLLGP2	1.14	1.2	1.26	V
AVDD12_PLLGP34	Analog power for PLLGP34	1.14	1.2	1.26	V
AVDD12_SSUSB	Analog power for SSUSB	1.14	1.2	1.26	V
AVDD12_USB_P0	Analog power for USB_P0	1.14	1.2	1.26	V
AVDD12_USB_P1	Analog power for USB_P1	1.14	1.2	1.26	V
AVDD12_USB_P2	Analog power for USB_P2	1.14	1.2	1.26	V

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Pin name	Description	Min.	Typ.	Max.	Unit
AVDD18_APU	Analog power for APU	1.71	1.8	1.89	V
AVDD18_AUXADC	Analog power for AUXADC	1.71	1.8	1.89	V
AVDD18_CKSQ	Analog power for CKSQ	1.71	1.8	1.89	V
AVDD18_DPTX	Analog power for DPTX	1.71	1.8	1.89	V
AVDD18_DSI	Analog power for DSI	1.71	1.8	1.89	V
AVDD18_EDPTX	Analog power for EDPTX	1.71	1.8	1.89	V
AVDD18_HDMITX21	Analog power for HDMITX21	1.71	1.8	1.89	V
AVDD18_PCIE	Analog power for PCIe	1.71	1.8	1.89	V
AVDD18_PLLGP1	Analog power for PLLGP1	1.71	1.8	1.89	V
AVDD18_PLLGP2	Analog power for PLLGP2	1.71	1.8	1.89	V
AVDD18_PLLGP34	Analog power for PLLGP34	1.71	1.8	1.89	V
AVDD18_PROC	Analog power for PROC	1.71	1.8	1.89	V
AVDD18_SSUSB	Analog power for SSUSB	1.71	1.8	1.89	V
AVDD18_USB_P0	Analog power for USB Port0	1.71	1.8	1.89	V
AVDD18_USB_P1	Analog power for USB Port1	1.71	1.8	1.89	V
AVDD18_USB_P2	Analog power for USB Port2	1.71	1.8	1.89	V
AVDD33_USB_P0	Analog power for USB Port0	2.92	3.07	3.22	V
AVDD33_USB_P1	Analog power for USB Port1	2.92	3.07	3.22	V
AVDD33_USB_P2	Analog power for USB Port2	2.92	3.07	3.22	V
AVDD075_EMI0	Analog power for EMI0	0.7125	0.75	0.7875	V
AVDD075_EMI2	Analog power for EMI2	0.7125	0.75	0.7875	V
AVDD12_EMI0	Analog power for EMI0	1.14	1.2	1.26	V
AVDD12_EMI2	Analog power for EMI2	1.14	1.2	1.26	V
AVDD18_EMI0	Analog power for EMI0	1.71	1.8	1.89	V
AVDD18_EMI2	Analog power for EMI2	1.71	1.8	1.89	V
AVDD2_EMI0 (LPDDR4X)	Analog power for EMI0 (LPDDR4X)	1.045	1.1	1.155	V
AVDD2_EMI0 (LPDDR4)	Analog power for EMI0 (LPDDR4)	1.045	1.1	1.155	V
AVDD2_EMI0 (DDR4)	Analog power for EMI0 (DDR4)	1.14	1.2	1.26	V
AVDD2_EMI2 (LPDDR4X)	Analog power for EMI2 (LPDDR4X)	1.045	1.1	1.155	V
AVDD2_EMI2 (LPDDR4)	Analog power for EMI2 (LPDDR4)	1.045	1.1	1.155	V
AVDD2_EMI2 (DDR4)	Analog power for EMI2 (DDR4)	1.14	1.2	1.26	V
AVDDQ_EMI0 (LPDDR4X)	Analog power for EMI0 (LPDDR4X)	0.57	0.6	0.63	V
AVDDQ_EMI0 (LPDDR4)	Analog power for EMI0 (LPDDR4)	1.045	1.1	1.155	V
AVDDQ_EMI0 (DDR4)	Analog power for EMI0 (DDR4)	1.14	1.2	1.26	V
AVDDQ_EMI2 (LPDDR4X)	Analog power for EMI2 (LPDDR4X)	0.57	0.6	0.63	V
AVDDQ_EMI2 (LPDDR4)	Analog power for EMI2 (LPDDR4X)	1.045	1.1	1.155	V
AVDDQ_EMI2 (DDR4)	Analog power for EMI2 (DDR4)	1.14	1.2	1.26	V
DVDD_ADSP	Digital power input for ADSP	0.71	0.75	0.81	V
DVDD_APU	Digital power input for APU	0.53	0.75	0.84	V
DVDD_CORE	Digital power input for Vcore	0.52	0.75	0.81	V
DVDD_GPU	Digital power input for GPU	0.55	0.75	0.86	V
DVDD_MM	Digital power input for ISP	0.52	0.75	0.81	V
DVDD_PROC_B	Digital power input for Big Core	0.52	0.75	1.19	V
DVDD_PROC_L	Digital power input for Little Core	0.52	0.75	0.97	V
DVDD_SRAM_APU	Digital power input for APU SRAM	0.71 0.57+	0.75	0.86	V
DVDD_SRAM_CORE	Digital power input for Core SRAM	0.71 0.57+	0.75	0.81	V
DVDD_SRAM_GPU	Digital power input for GPU SRAM	0.71	0.85	0.92	V

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Pin name	Description	Min.	Typ.	Max.	Unit
		0.57+			
DVDD_SRAM_MM	Digital power input for ISP SRAM	0.71 0.57+	0.75	0.81	V
DVDD_SRAM_PROC_B	Digital power input for Big Core SRAM	0.71 0.57+	0.85	1.19	V
DVDD_SRAM_PROC_L	Digital power input for Little Core SRAM	0.71 0.57+	0.85	1.08	V
DVDD18_IODPI	Digital power input for I/O	1.71	1.8	1.89	V
DVDD18_IOEMMC	Digital power input for I/O	1.71	1.8	1.89	V
DVDD18_IOLM	Digital power input for I/O	1.71	1.8	1.89	V
DVDD18_IOLT	Digital power input for I/O	1.71	1.8	1.89	V
DVDD18_IORM	Digital power input for I/O	1.71	1.8	1.89	V
DVDD18_IORT	Digital power input for I/O	1.71	1.8	1.89	V
DVDD18_MSDC1	Digital power input for I/O	1.71	1.8	1.89	V
DVDD18_MSDC2	Digital power input for I/O	1.71	1.8	1.89	V
DVDD28_IODPI	Digital power input for DPI	1.71	3	3.15	V
DVDD28_MSDC1	Digital power input for MSDC1	1.71	3	3.15	V
DVDD28_MSDC2	Digital power input for MSDC2	1.71	3	3.15	V

Note: The values with "+" sign are for SRAM retention only, not for operation.

5.3 DC Electrical Specifications

This section provides DC electrical characteristics per buffer type.

5.3.1 PMIC_RTC32K_CK DC Specifications

Table 5-4 PMIC_RTC32K_CK DC specifications

Parameter		Min.	Typ.	Max.	Unit
Operating voltage = 1.8 V					
INPUT					
V_{IH}	Input logic high voltage	0.65 × VDDIO(1)		VDDIO(1) + 0.3	V
V_{IL}	Input logic low voltage	-0.3		0.35 × VDDIO(1)	V
F_{RTC}	Input clock frequency		32		kHz
DC_{RTC}	Input signal duty cycle	45	50	55	%
OUTPUT					
V_{OH}	DC output logic high voltage	0.75 × VDDIO(1)			V
V_{OL}	DC output logic low voltage			0.25 × VDDIO(1)	V

1. VDDIO in this table stands for corresponding power supply (i.e. DVDD18_IOLT). For more information on the power supply name on the corresponding ball, see Table 4-19 Pin characteristics, *Power Domain* column.

5.3.2 SPII2CUARTIO DC Electrical Specifications

Table 5-5 SPII2CUARTIO DC specifications

Parameter	Min.	Typ.	Max.	Unit
Operating voltage = 1.8 V				
INPUT				

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Parameter		Min.	Typ.	Max.	Unit
V_{IH}	Input logic high voltage	0.65 × VDDIO[1]		VDDIO + 0.3	V
V_{IL}	Input logic low voltage	-0.3		0.35 × VDDIO[1]	V
OUTPUT					
V_{OH}	DC output logic high voltage	0.75 × VDDIO[1]			V
V_{OL}	DC output logic low voltage			0.25 × VDDIO[1]	V

1. VDDIO in this table stands for corresponding power supply (i.e. VDD18_IORM). For more information on the power supply name on the corresponding ball, see Table 4-19 Pin characteristics, *Power Domain* column.

5.3.3 I2C/I2SIO DC Specifications

Table 5-6 I2C/I2S DC specifications

Parameter		Min.	Typ.	Max.	Unit
Operating voltage = 1.8 V					
INPUT					
V_{IH}	Input logic high voltage	0.65 × VDDIO[1]		VDDIO[1] + 0.3	V
V_{IL}	Input logic low voltage	-0.3		0.35 × VDDIO[1]	V
OUTPUT					
V_{OH}	DC output logic high voltage	0.75 × VDDIO[1]			V
V_{OL}	DC output logic low voltage			0.25 × VDDIO[1]	V

1. VDDIO in this table stands for corresponding power supply (i.e. DVDD18_IOLT). For more information on the power supply name on the corresponding ball, see Table 4-19 Pin characteristics, *Power Domain* column.

5.3.4 I3CIO DC Specifications

Table 5-7 I3CIO DC specifications

Parameter		Min.	Typ.	Max.	Unit
Operating voltage = 1.8 V					
INPUT					
V_{IH}	Input logic high voltage	0.65 × VDDIO[1]		VDDIO[1] + 0.3	V
V_{IL}	Input logic low voltage	-0.3		0.35 × VDDIO[1]	V
OUTPUT					
V_{OL}	DC output logic low voltage			0.2 × VDDIO[1]	V

1. VDDIO in this table stands for corresponding power supply (i.e. DVDD18_IORT). For more information on the power supply name on the corresponding ball, see Table 4-19 Pin characteristics, *Power Domain* column.

5.3.5 eMMCIO DC Specifications

Table 5-8 eMMCIO DC specifications

Parameter		Min.	Typ.	Max.	Unit
Operating voltage = 1.8 V					
INPUT					
V_{IH}	Input logic high voltage	0.65 × VDDIO[1]		VDDIO[1] + 0.3	V
V_{IL}	Input logic low voltage	-0.3		0.35 × VDDIO[1]	V
OUTPUT					

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Parameter		Min.	Typ.	Max.	Unit
V_{OH}	DC output logic high voltage	1.4			V
V_{OL}	DC output logic low voltage			0.45	V

1. VDDIO in this table stands for corresponding power supply (i.e. DVDD18_IOEMMC). For more information on the power supply name on the corresponding ball, see Table 4-19 Pin characteristics, *Power Domain* column.

5.3.6 MSDC1IO DC Specifications

Table 5-9 MSDC1IO DC specifications (2.8V/3.0V)

Parameter		Min.	Typ.	Max.	Unit
Operating voltage = 2.8V/3.0V					
INPUT					
V_{IH}	Input logic high voltage	0.75 × VDDIO(1)		VDDIO(1) + 0.15	V
V_{IL}	Input logic low voltage	-0.3		0.25 × VDDIO(1)	V
OUTPUT					
V_{OH}	DC output logic high voltage	0.625 × VDDIO(1)		VDDIO(1) + 0.15	V
V_{OL}	DC output logic low voltage	-0.3		0.125 × VDDIO(1)	V

1. VDDIO in this table stands for corresponding power supply (i.e. DVDD28_MSDC1). For more information on the power supply name on the corresponding ball, see Table 4-19 Pin characteristics, *Power Domain* column.

Table 5-10 MSDC1IO DC specifications

Parameter		Min.	Typ.	Max.	Unit
Operating voltage = 1.8 V					
INPUT					
V_{IH}	Input logic low voltage	0.7 × VDDIO(1)		VDDIO(1) + 0.15	V
V_{IL}	Input logic high voltage	-0.3		0.3 × VDDIO(1)	V
OUTPUT					
V_{OH}	DC output logic high voltage	1.4		VDDIO(1) + 0.15	V
V_{OL}	DC output logic low voltage	-0.3		0.45	V

1. VDDIO in this table stands for corresponding power supply (i.e. DVDD28_MSDC1). For more information on the power supply name on the corresponding ball, see Table 4-19 Pin characteristics, *Power Domain* column.

5.3.7 MSDC2IO DC Specifications

Table 5-11 MSDC2IO DC specifications (2.8V/3.0V)

Parameter		Min.	Typ.	Max.	Unit
Operating voltage = 2.8V/3.0V					
INPUT					
V_{IH}	Input logic high voltage	0.75 × VDDIO(1)		VDDIO(1) + 0.15	V
V_{IL}	Input logic low voltage	-0.3		0.25 × VDDIO(1)	V
OUTPUT					
V_{OH}	DC output logic high voltage	0.625 × VDDIO(1)		VDDIO(1) + 0.15	V
V_{OL}	DC output logic low voltage	-0.3		0.125 × VDDIO(1)	V

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1. VDDIO in this table stands for corresponding power supply (i.e. DVDD28_MSDC2). For more information on the power supply name on the corresponding ball, see Table 4-19 Pin characteristics, *Power Domain* column.

Table 5-12 MSDC2IO DC

Parameter		Min.	Typ.	Max.	Unit
Operating voltage = 1.8 V					
INPUT					
V_{IH}	Input logic high voltage	0.7 × VDDIO(1)		VDDIO(1) + 0.15	V
V_{IL}	Input logic low voltage	-0.3		0.3 × VDDIO(1)	V
OUTPUT					
V_{OH}	DC output logic high voltage	1.4		VDDIO(1) + 0.15	V
V_{OL}	DC output logic low voltage	-0.3		0.45	V

1. VDDIO in this table stands for corresponding power supply (i.e. DVDD28_MSDC2). For more information on the power supply name on the corresponding ball, see Table 4-19 Pin characteristics, *Power Domain* column.

5.4 Power Management

5.4.1 Power Sequence

Refer to PMIC datasheet for detailed timing sequence.

5.5 Reset

The TOPRGU generates reset signals and distributes them to each system. A WDT is also included in this module.

The TOPRGU supports the following features:

- Hardware reset signals for the whole chip
- Software controllable reset
- WDT
- Reset output signals for companion chips

Figure 5-1 shows the block diagram of TOPRGU in MT8390.

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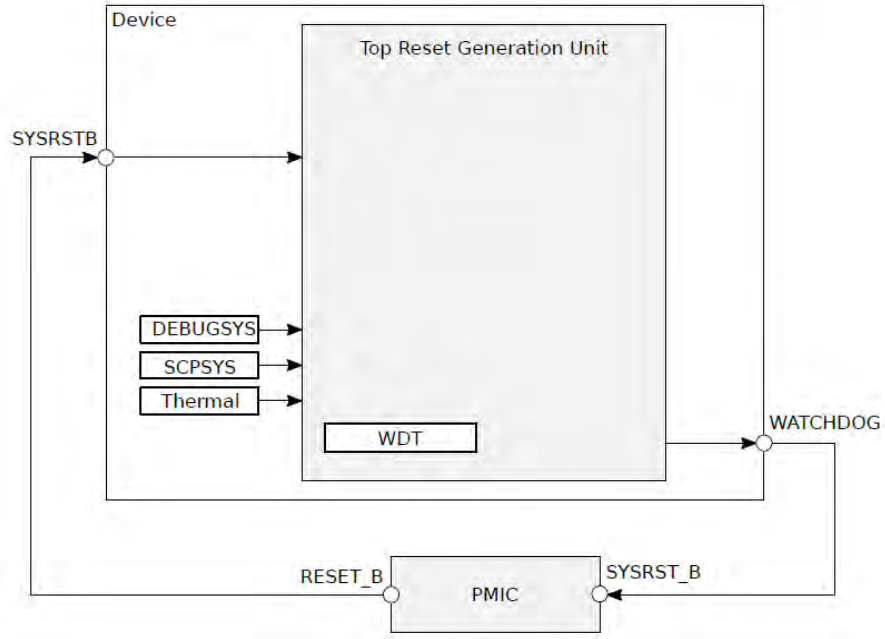

Figure 5-1 Reset block diagram

5.5.1 Reset Signal Descriptions

Table 5-13 presents Reset signal description.

Table 5-13 Reset signal descriptions

Signal name	Type	Description	Ball location
SYSRSTB	DI	System reset input	T32
WATCHDOG	DO	Watchdog reset output	K34

5.6 DSI Specifications

Table 5-14 presents MIPI D-PHY TX electrical characteristics.

Table 5-14 DSI D-PHY TX electrical characteristics

Description	Min.	Typ.	Max.	Unit	Note
High-Speed data rate	125	-	1200	Mbps	
High-Speed common mode voltage	150	200	250	mV	
High-Speed differential output voltage	140	200	270	mV	
High-Speed single ended output high voltage	-	-	360	mV	
High-Speed single ended output impedance	40	50	62.5	Ω	
High-Speed 20%-80% rise time and fall time	-	-	0.3	UI	1
	-	-	0.35	UI	2
	100	-	-	ps	3
Low-Power output high level	0.95	1.2	1.3	V	
Low-Power output low level	-50	-	50	mV	
Low-Power output impedance	110	-	-	Ω	
Low-Power 15%-85% rise time and fall time	-	-	25	ns	

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Note:

1. Applicable when supporting maximum HS bit rates ≤ 1 Gbps (UI ≥ 1 ns)
2. Applicable when supporting maximum HS bit rates > 1 Gbps (UI ≤ 1 ns) but less than ≤ 1.5 Gbps
3. Applicable when supporting maximum HS bit rates ≤ 1.5 Gbps

Table 5-15 presents MIPI C-PHY TX electrical characteristics.

Table 5-15 DSI C-PHY TX electrical characteristics

Description	Min.	Typ.	Max.	Unit	Note
High-Speed symbol rate	125	-	1100	Msps	
High-Speed common mode voltage	175	225 to 250	310	mV	
High-Speed differential output voltage of strong one	-	-	300	mV	
High-Speed differential output voltage of weak one	97	-	-	mV	
High-Speed single ended output high voltage	-	-	425	mV	
High-Speed single ended output impedance	40	50	60	Ω	
High-Speed rise time and fall time from -58mV to 58mV	-	-	0.4	UI	
Low-Power output high level	0.95	1.2	1.3	V	
Low-Power output low level	-50	-	50	mV	
Low-Power output impedance	110	-	-	Ω	
Low-Power 15%-85% rise time and fall time	-	-	25	ns	

5.7 CSI-2 Specifications

Electrical characteristics are compatible with MIPI D-PHY Specification Revision 1.2.

Table 5-16 CSI D-PHY RX electrical characteristics

Description	Min.	Typ.	Max.	Unit	Note
High-Speed data rate	80	-	2500	Mbps	
High-Speed common point voltage	70	-	330	mV	
High-Speed differential input high voltage	-	-	40	mV	
High-Speed differential input low voltage	-40	-	-	mV	
High-Speed single ended input high voltage	-	-	460	mV	
High-Speed single ended input low voltage	-40	-	-	mV	
High-Speed differential input impedance	80	100	125	Ω	
Low-Power logic 1 input voltage	740	-	-	mV	
Low-Power logic 0 input voltage	-	-	550	mV	
Low-Power input hysteresis	25	-	-	mV	
Minimum pulse width response	20	-	-	ns	

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6 Clock Characteristics

The device has two external input clocks—low frequency (RTC32K_CK) and high frequency (X26M_IN). Figure 6-1 shows the external clock sources and clock outputs.

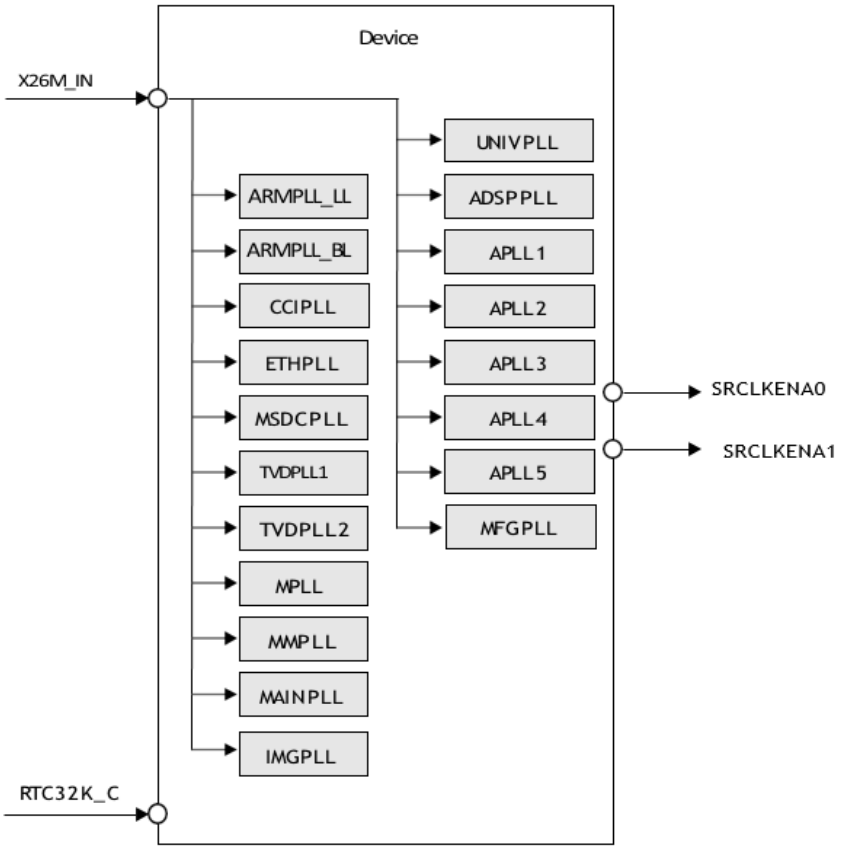

Figure 6-1 Device clock diagram

6.1 Maximum Performance Ratings

Table 6-1 presents the maximum core and peripheral performance limitations and correlations.

Table 6-1 Maximum performance ratings

Module		Max.	Unit
Quad-core Arm Cortex-A78	A78	2200	MHz
Quad-core Arm Cortex-A55	A55	2000	MHz
Graphics Accelerator	GPU	950	MHz
HiFi 5 DSP	DSP	800	MHz
AI Processor Unit	APU	832	MHz
System Companion Processor	SCP	832	MHz
External Memory Interface	LPDDR4(X)	3733	Mbps
	DDR4	3200	Mbps
Memory Card Controller	SD Card	100	MBps
	eMMC	400	MBps
	SDIO	100	MBps
Serial NOR Flash Interface	SNOR	52	MHz

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Module		Max.	Unit
Digital Display Parallel Interface	DPI	148	MHz
High-Definition Multimedia Interface Transmitter	HDMITX	594	MHz
DisplayPort	DPTX	5.4	Gbps/lane
Embedded DisplayPort Interface	EDPTX	5.4	Gbps/lane
Display Serial Interface	DSI D-PHY	1.5	Gbps/lane
	DSI C-PHY	1.1	Gsps/trio
Image Signal Processor	ISP	32	MPix@30fps
Camera Serial Interface 2	CSI D-PHY	2.5	Gbps/lane
	CSI C-PHY	4.5	Gsps/trio
Video Encoder	VENC	624	MHz
Video Decoder	VDEC	594	MHz
Inter-IC Sound	I2S master mode (sampling frequency)	192	kHz
	I2S slave mode (sampling frequency)	192	kHz
Programmable Command Master Interface	PCM (sampling frequency)	48	kHz
Pulse Density Modulation	PDM	3.25	MHz
Time Division Multiplexed Interface	TDM (sampling frequency)	48	kHz
Digital Interface	SPDIF	192	kHz
Inter-Integrated Circuit	I2C mode	3.4	Mbps
	I3C mode	12.5	Mbps
Universal Asynchronous Receiver/Transmitter	UART	961,200	bps
Serial Peripheral Interface	SPI master	52	MHz
Universal Serial Bus	USB SuperSpeed	5	Gbps
	USB High-Speed	480	Mbps
	USB Full-Speed	12	Mbps
	USB Low-Speed	1.5	Mbps
Ethernet Network Interface Controller	MII	25	MHz
	RMII	50	MHz
	RGMII	125	MHz
Peripheral Component Interconnect Express	PCIe	8.0	GT/s
Pulse Width Modulation	PWM	39	MHz
Auxiliary ADC	AUXADC (clock rate)	3.25	MHz

6.2 PLL Spec

Table 6-2 shows ARMPLL_LL specifications.

Table 6-2 ARMPLL_LL specifications

Parameter		Min.	Typ.	Max.	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		2000		MHz

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Parameter		Min.	Typ.	Max.	Unit
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	45	50	55	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			100	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-3 shows ARMPLL_BL specifications.

Table 6-3 ARMPLL_BL specifications

Parameter		Min.	Typ.	Max.	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		2252.25		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	45	50	55	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			100	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-4 shows CCIPLL specifications.

Table 6-4 CCIPLL specifications

Parameter		Min.	Typ.	Max.	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		1600		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	45	50	55	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			100	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-5 shows ETHPLL specifications.

Table 6-5 ETHPLL specifications

Parameter		Min.	Typ.	Max.	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		500		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	45	50	55	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			100	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-6 shows MSDCPLL specifications.

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Table 6-6 MSDCPLL specifications

Parameter		Min.	Typ.	Max.	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		416.14648		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	45	50	55	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			100	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-7 shows TVDPLL1 specifications.

Table 6-7 TVDPLL1 specifications

Parameter		Min.	Typ.	Max.	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		594.177		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	45	50	55	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			100	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-8 shows TVDPLL2 specifications.

Table 6-8 TVDPLL2 specifications

Parameter		Min.	Typ.	Max.	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		594.177		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	45	50	55	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			100	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-9 shows MPLL specifications.

Table 6-9 MPLL specifications

Parameter		Min.	Typ.	Max.	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		208.03		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	45	50	55	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			100	ps
DVDD	Digital power supply	0.54	0.8	0.88	V

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Parameter		Min.	Typ.	Max.	Unit
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-10 shows MMPLL specifications.

Table 6-10 MMPLL specifications

Parameter		Min.	Typ.	Max.	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		2750.048		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	45	50	55	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			100	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-11 shows MAINPLL specifications.

Table 6-11 MAINPLL specifications

Parameter		Min.	Typ.	Max.	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		2184.359		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	45	50	55	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			100	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-12 shows IMGPLL specifications.

Table 6-12 IMGPLL specifications

Parameter		Min.	Typ.	Max.	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		660		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	45	50	55	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			100	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-13 shows UNIVPLL specifications.

Table 6-13 UNIVPLL specifications

Parameter		Min.	Typ.	Max.	Unit
F_{IN}	Input clock frequency		26		MHz

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Parameter		Min.	Typ.	Max.	Unit
F_{OUT}	Output clock frequency		2496.006		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	45	50	55	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			100	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-14 shows ADSPPLL specifications.

Table 6-14 ADSPPLL specifications

Parameter		Min.	Typ.	Max.	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		800		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	45	50	55	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			100	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-15 shows APLL1 specifications.

Table 6-15 APLL1 specifications

Parameter		Min.	Typ.	Max.	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		196.001		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	45	50	55	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			100	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-16 shows APLL2 specifications.

Table 6-16 APLL2 specifications

Parameter		Min.	Typ.	Max.	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		196.001		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	45	50	55	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			100	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

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Table 6-17 shows APLL3 specifications.

Table 6-17 APLL3 specifications

Parameter		Min.	Typ.	Max.	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		196.001		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	45	50	55	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			100	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-18 shows APLL4 specifications.

Table 6-18 APLL4 specifications

Parameter		Min.	Typ.	Max.	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		196.001		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	45	50	55	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			100	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-19 shows APLL5 specifications.

Table 6-19 APLL5 specifications

Parameter		Min.	Typ.	Max.	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		196.001		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	45	50	55	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			100	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-20 shows MFGPLL specifications.

Table 6-20 MFGPLL specifications

Parameter		Min.	Typ.	Max.	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		390		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	45	50	55	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			100	ps

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Parameter		Min.	Typ.	Max.	Unit
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

6.3 Clock Squarer

The Clock Squarer (CKSQ) is designed to receive clock signal from pin “X26M_IN” and distribute it to the chip internally.

Table 6-21 shows the CKSQ specifications.

Table 6-21 CKSQ specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IN}	Input signal amplitude	1,000	1,200	1,250	mVpp
D_{cycIN}	Input signal duty cycle		50		%
D_{cycOUT}	Output signal duty cycle	D_{cycIN} - 5		D_{cycIN} + 5	%
	Maximum positive overshoot			1.3	V
	Minimum negative overshoot	-0.1			V

6.4 Clock Signal Descriptions

Table 6-22 Clock signal descriptions

Signal name	Type	Description	Ball location
RTC32K_CK	DI	RTC 32kHz clock input	N37
X26M_IN	AI	26 MHz clock input	AE34
SRCLKENA0	DO	Output signal; control of PMIC 26 MHz / Buck / LDO normal mode or sleep High: Normal mode Low: Sleep mode or low power mode	L33
SRCLKENA1	DO	Output signal; control of PMIC 26 MHz / Buck / LDO on or off	L34

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7 Package Information

7.1 Thermal Specifications

7.1.1 Thermal Operating Specifications

Table 7-1 presents the thermal resistance characteristics and maximum operating temperatures of the device.

Table 7-1 Thermal operating specifications

Symbol	Description	Value	Unit
T_j	Max. operating junction temperature	105	°C
θ_{JA}	Package thermal resistances in natural convection	21.8	°C/Watt
θ_{JB}	Package thermal resistances of junction-to-board	4.5	°C/Watt
θ_{JC}	Package thermal resistances of junction-to-case	2.85	°C/Watt

7.2 Top Marking

Figure 7-1 shows the device top marking definition.

Figure 7-1 Top marking

Table 7-2 presents the printed device reference and decoding.

Table 7-2 Printed device reference and decoding

Parameter		Value	Description
NNNNNN#N	Part number	MT8390#V	Product family
#:	Function code 1		For internal use only
YYWW	Date code		2-digits year and week code
&&&&&	Lot number		For internal use only
%	Function code 2		For internal use only
O	Pin one designator		Pin one location

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7.3 Mechanical Drawing

The following figure shows printed device reference diagram (MFC VFBGA 15.0 mm × 15.0 mm, 1204-ball, 0.4 mm pitch package).

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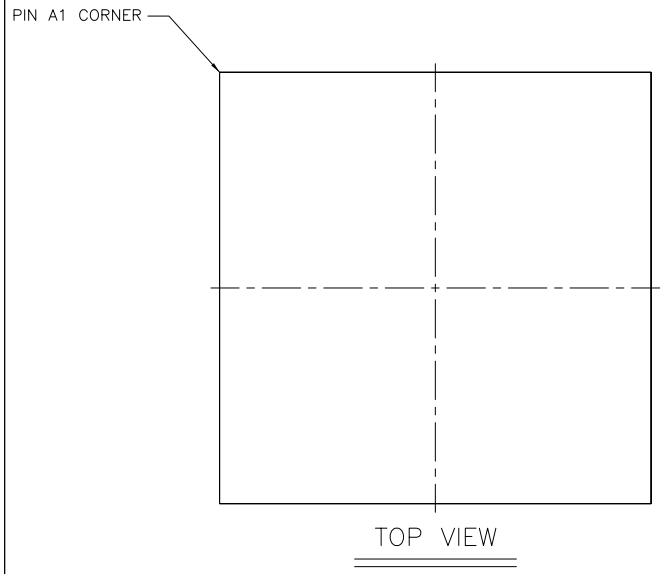

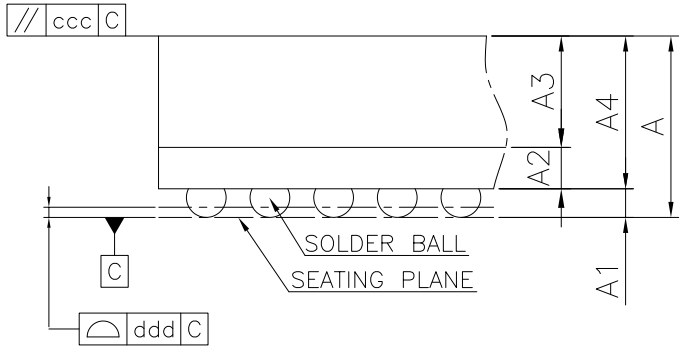

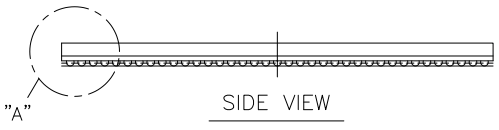

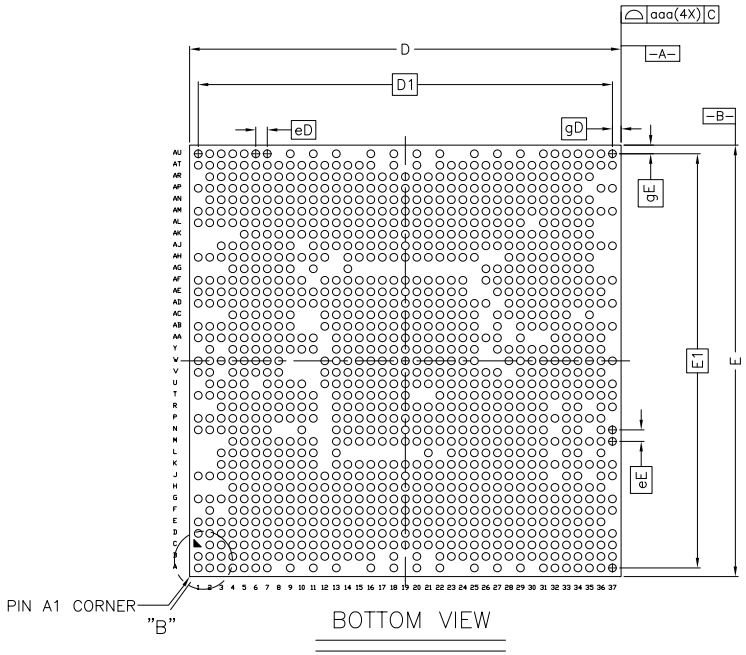

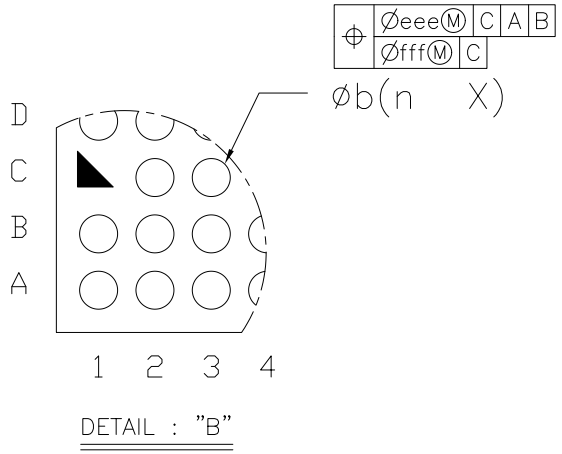

Item		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package Type			MFC VFBGA		
Body Size	X	D	14.950	15.000	15.050
	Y	E	14.950	15.000	15.050
Ball Pitch	X	eD		0.400	
	Y	eE		0.400	
Mold Thickness		A3		0.450 Ref.	
Substrate Thickness		A2		0.168 Ref.	
Substrate+Mold Thickness		A4	0.568	0.618	0.668
Total Thickness		A	–	–	0.900
Ball Diameter				0.250	
Ball Stand Off		A1	0.140	0.180	0.220
Ball Width		b	0.220	0.270	0.320
Package Edge Tolerance		aaa		0.050	
Mold Flatness		ccc		0.150	
Coplanarity		ddd		0.100	
Ball Offset (Package)		eee		0.150	
Ball Offset (Ball)		fff		0.050	
Ball Count		n		1204	
Edge Ball Center to Center	X	D1		14.400	
	Y	E1		14.400	
Edge Ball Center to Package Edge	X	gD		0.300	
	Y	gE		0.300	

TITLE	PACKAGE OUTLINE		
	MFC VFBGA 1204L 15 X 15 X 0.9mm		
DWG. NO.	REV.	SHEET	UNIT
MT-AP01693	A	1 OF 2	MM

8 Legal and Support Information

8.1 Related Documents and Products

Documents:

- **MMD (MediaTek Module Design)—**Power Delivery Network (PDN) and DRAM design implementation solutions
- **MT8390 Baseband Design Notice—**Application note including schematic examples for peripheral interfaces such as GPIO, MSDC, SPI NOR, LPDDR4X, I2C/I3C, SPI, Display, Camera, USB, DPI, Ethernet, HDMI, PCIe, Audio, and power design implementation recommendations.
- **MT6319 Application Note for MT8390—**MediaTek MT6319 PMIC application note covering functional description and PCB layout guidelines.
- **MT6365 Application Note for MT8390—**MediaTek MT6365 PMIC application note covering functional description and PCB layout guidelines.
- **MT6680 Application Note for MT8390—**MediaTek MT6680 PMIC application note covering functional description and PCB layout guidelines.
- **MA5721F Application Note for MT8390—**MediaTek MA5721F PMIC application note covering functional description and PCB layout guidelines.

Companion chips:

- **MT6319—**Integrated Power Management IC (PMIC)
- **MT6365—**Integrated Power Management IC
- **MT6680—**Integrated Power Management IC
- **MA5721F—**Integrated Power Management IC

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