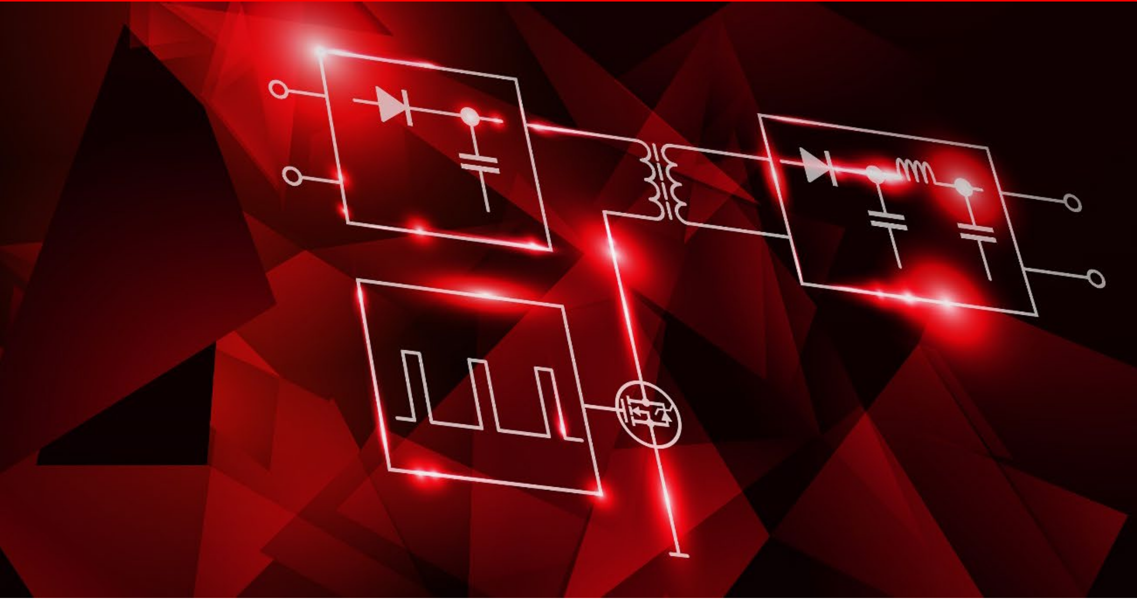


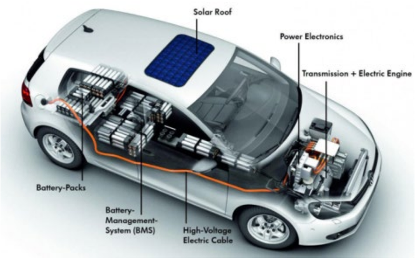
RUTRONIK TechTalk meets Gate Driver

DC/DCs for isolated gate drivers for e-mobility applications

Steve Roberts | Innovation Manager

RECOM Engineering GmbH & Co. KG

What do all these applications have in common?-they all use high frequency switchers



Advantages of Fast Switching

RECOM

- Improved power density

(smaller components)

- Higher efficency

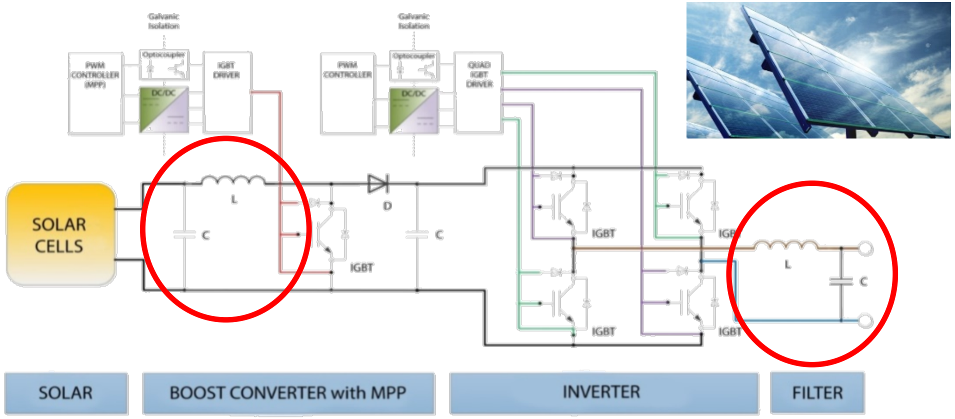
(over a wider input voltage range)

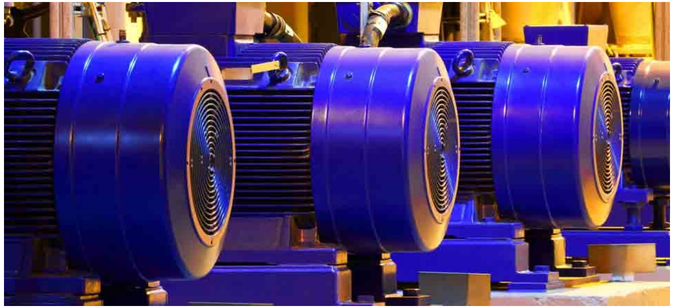
- More precise control

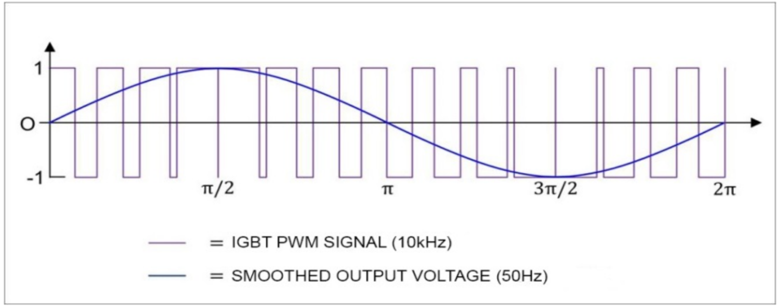
(faster response)

- Avoid AM Radio Band

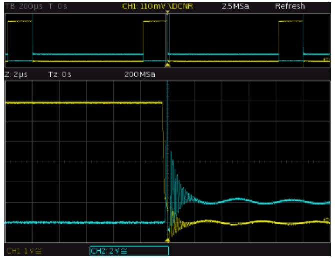
(535-1605kHz)

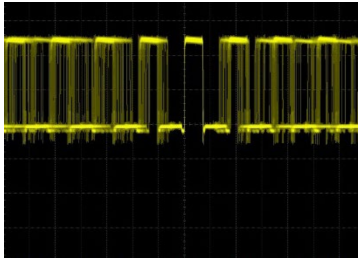






Disadvantages of Fast Switching





- Higher peak voltages (EMI problems?)
- High dv/dt stress on components (Lifetime?)
- High di/dt makes layout critical (Hidden costs?)
- Switching reliability and stability (1st. Pulse?)

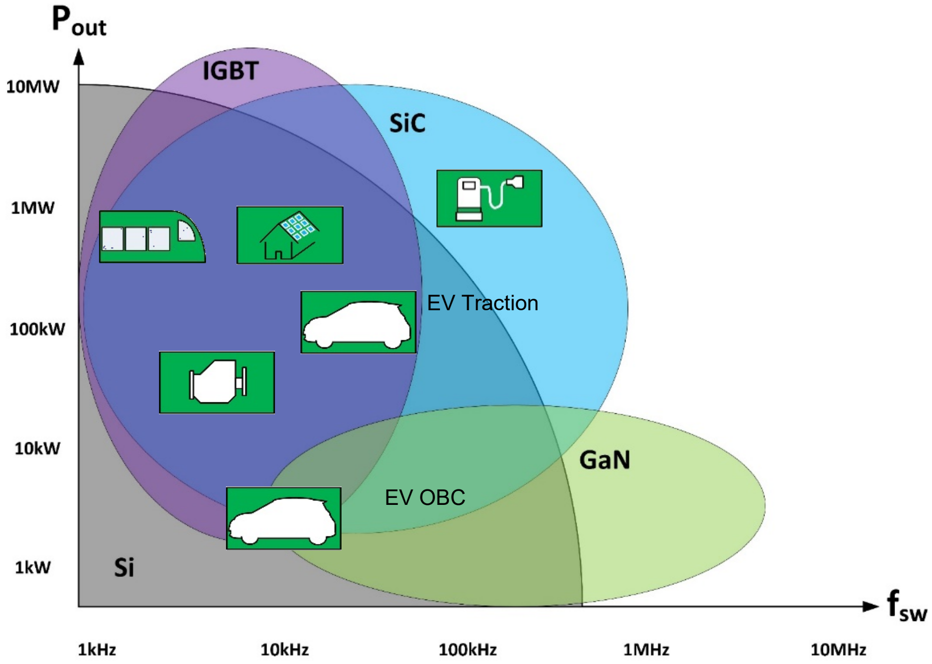
(Analogy: racehorse vs carthorse)

Power/Switching Freq. Comparison

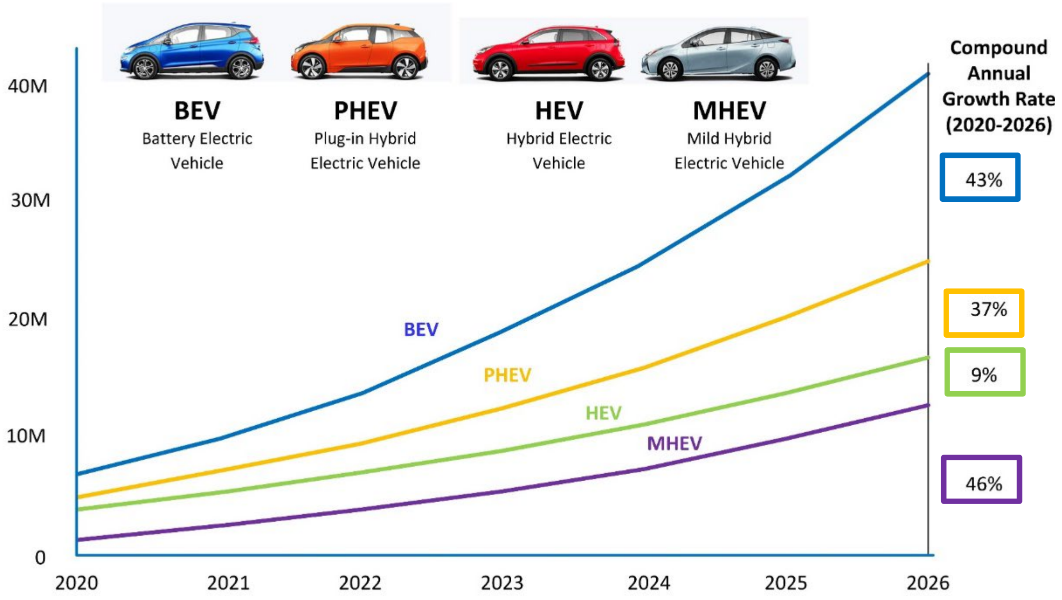
Type	f_{max}
Si	100kHz @ 100kW
SiC	1MHz @ 100kW
GaN	3MHz @ 3kW

$$f_{max} = \frac{1}{t_d + t_r + t_s + t_f}$$

Switch on:
Delay time (t_d) - how long it takes to get out of cutoff
Rise time (t_r) - transition from cutoff to saturation
Switch off:
Storage time (t_s) - how long to get out of saturation
Fall time (t_f) - transition from saturation to cutoff



Hybrid/Battery Electric Vehicles



2nd. Gen. BEV, PHEV, HEV
„800V“ (650 – 920V)

1200V Transistors

1st. Gen. BEV, PHEV, HEV
„400V“ (200-450V)

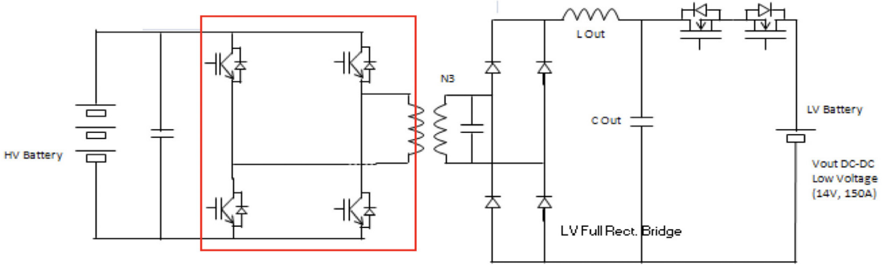
900V Transistors

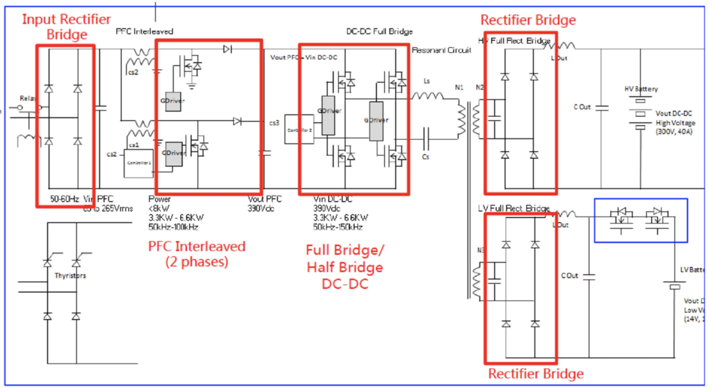
MHEV
„48V“ (20-60V)

100V Transistors

E-mobility Applications

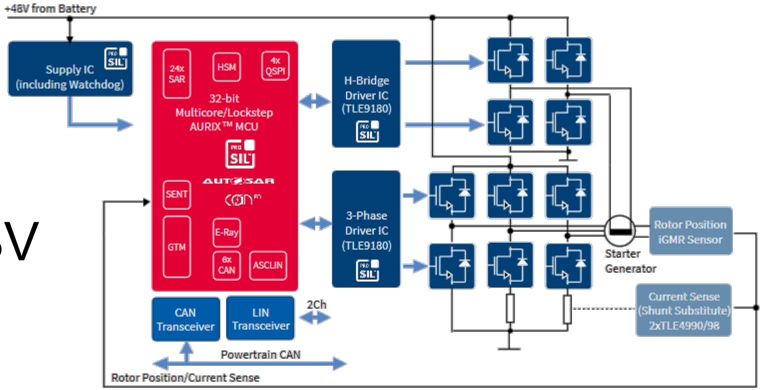
On-Board DC/DC

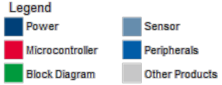




On-Board Charger

Microhybrid 48V Powertrain

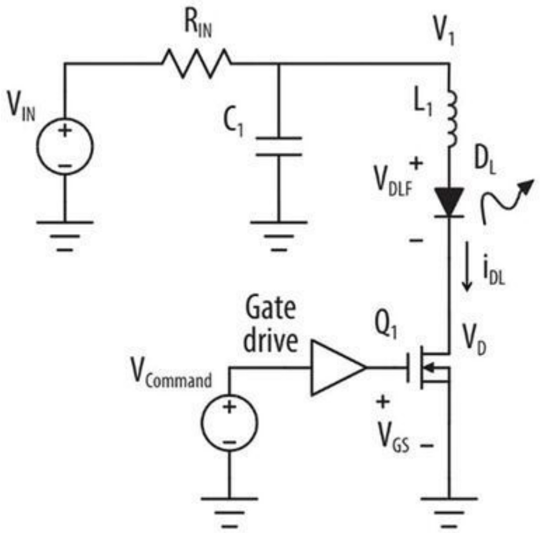


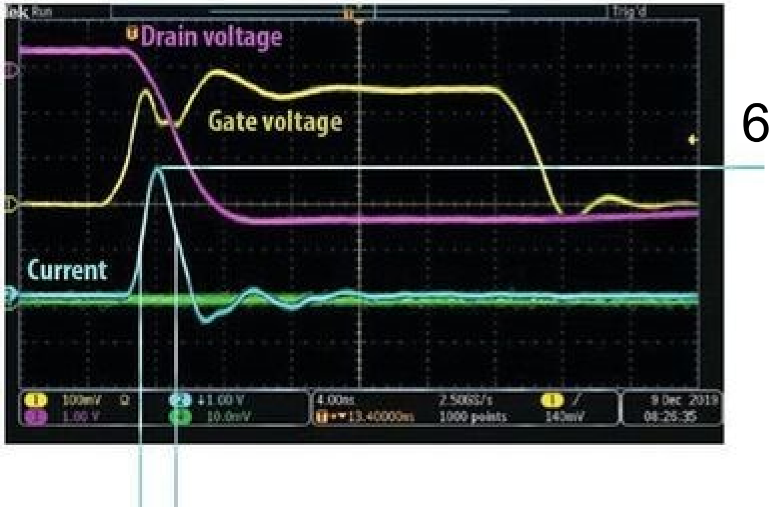


https://rutronik-tec.com/rutronik-automotive-drive-train/infineon-powertrain-48v-application-microhybrid/

E-mobility Applications

LIDAR (capacitive discharge laser driver)

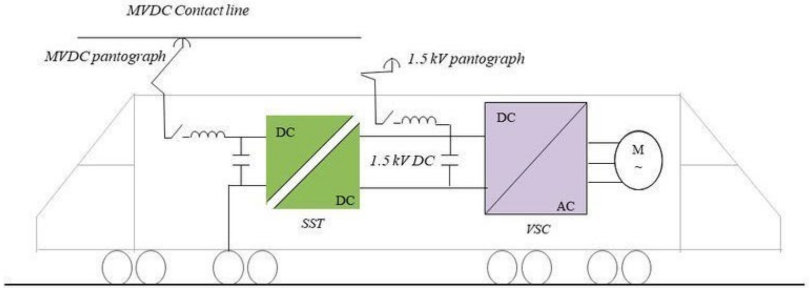


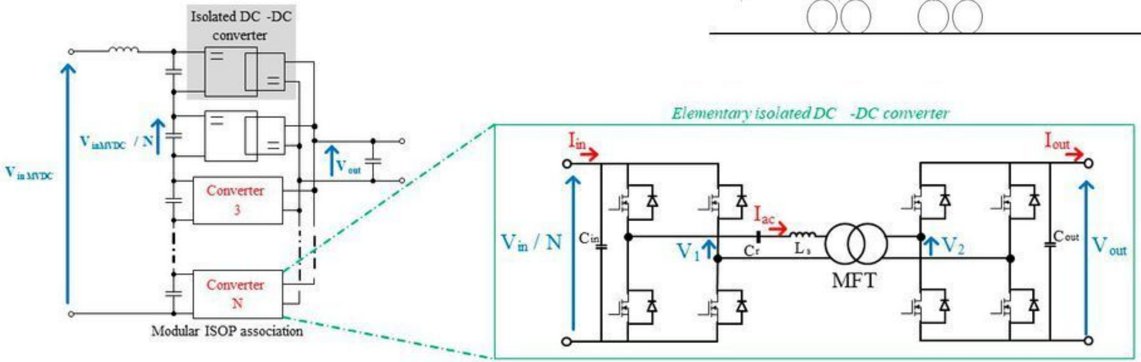


60A peak

4ns pulse width

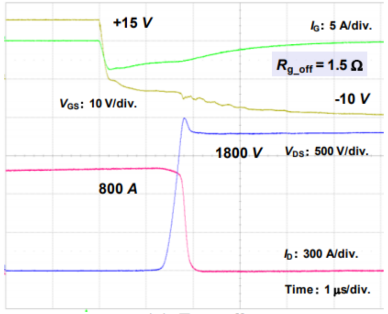
Railway „Solid-State Transformer"



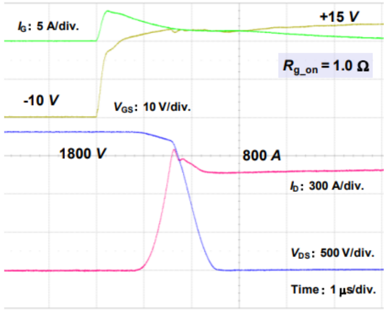


Design Considerations for High Frequency Switching

- Design Issues for the Gate Driver Circuit
- Which WBG Transistor?
- Isolated Power for the Gate Driver



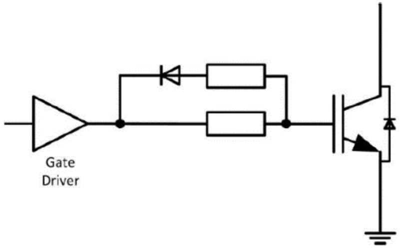
(a) Turn-off

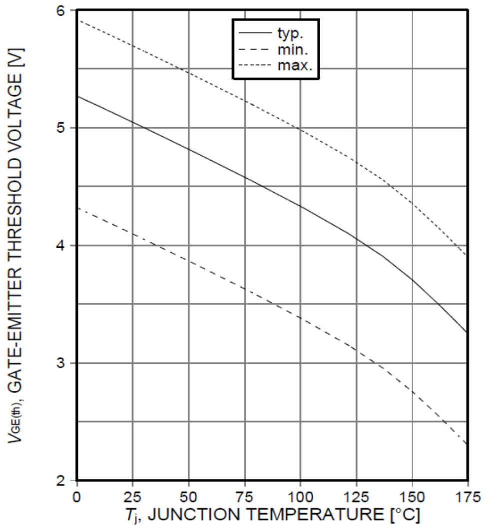


(b) Turn-on

Design Considerations for High Frequency Switching: Gate Threshold Voltage

The gate threshold voltage, V_{TH} , is typically 2-4 volts above the emitter/source terminal voltage, with some variation between components and over temperature:





Gate-emitter threshold voltage as a function of junction temperature
(I_C=0.29mA)

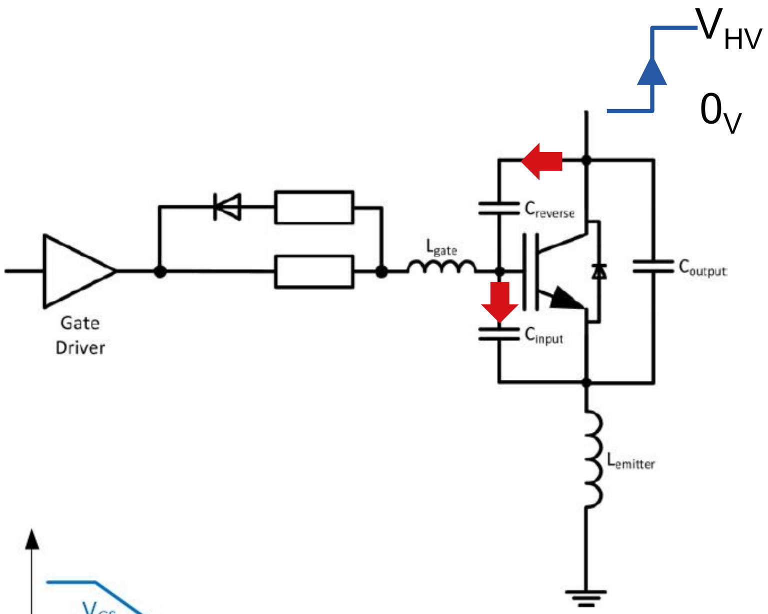
If there is no gate drive, the transistor is clearly off, but many datasheets recommend a negative gate drive „for safety". Why?

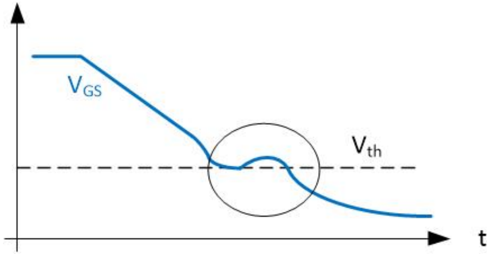
Why Negative Gate Drive?

False turn-on via gate capacitance ($C_{reverse}$ or C_{Miller})

High turn-off dv/dt causes current to flow through $C_{reverse}$ which charges up C_{input} forcing V_{gate} to rise.

Worst case: the transistor turns back on again!



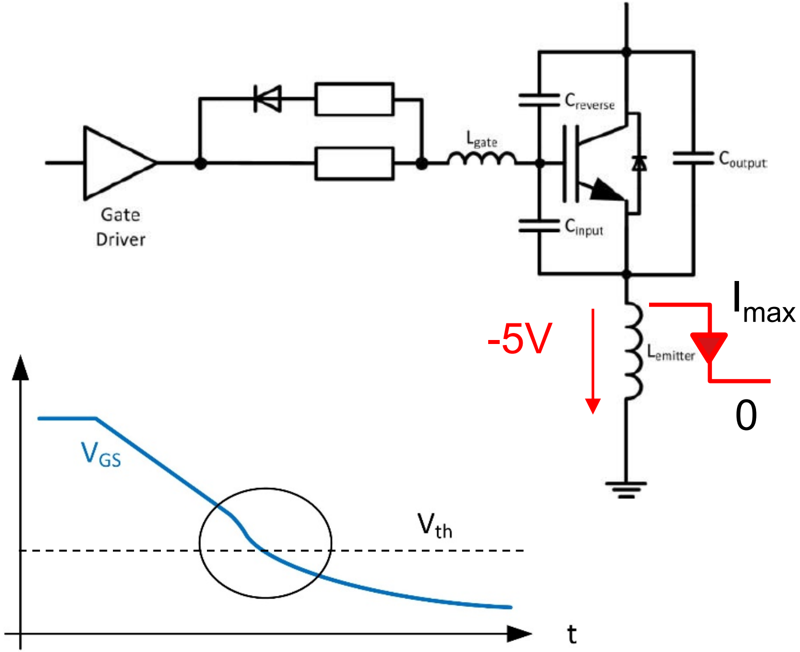


Why Negative Gate Drive?

False turn-on via „ground bounce“ across $L_{emitter}$

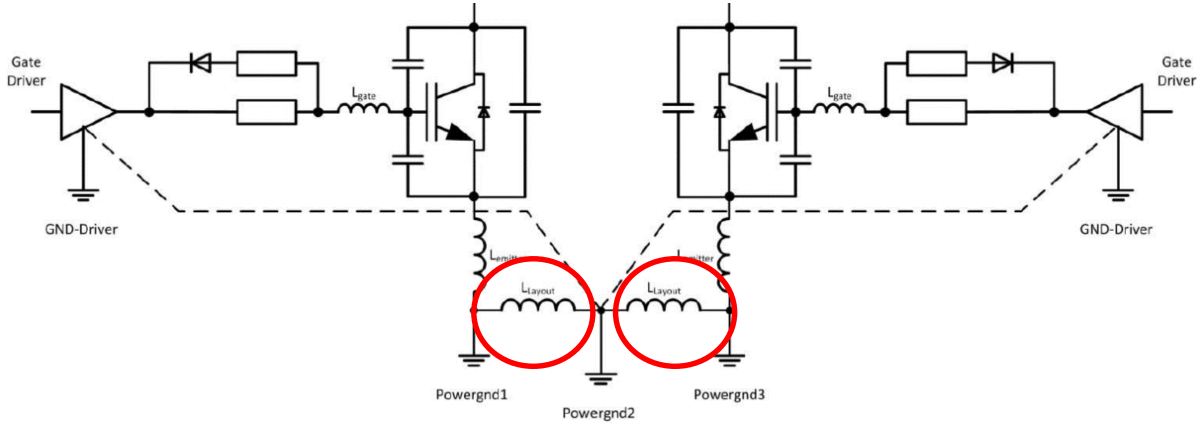
High di/dt induces a voltage across any layout inductances: -V= L*di/dt
e.g. If $L_{emitter}$ =5 nH
(inductance of 5mm PCB track) then:
-V= 5nH *1000A/µs = - 5 V

Worst case: the transistor turns back on again!



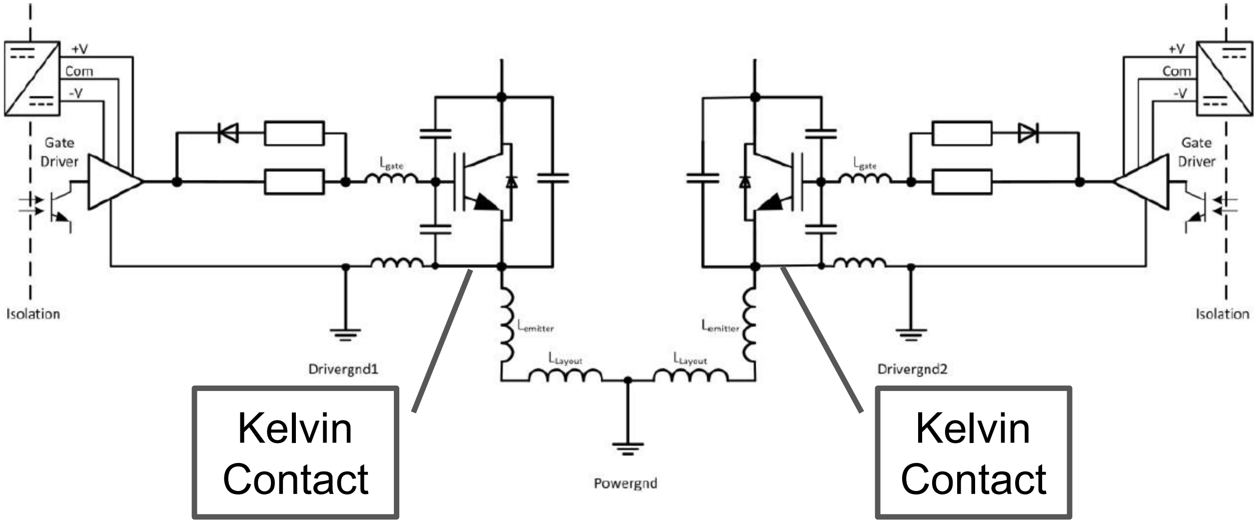
Layout Parasitic Inductance

Any imbalance in the layout parasitics can cause an imbalance in the switching behaviours of each leg :



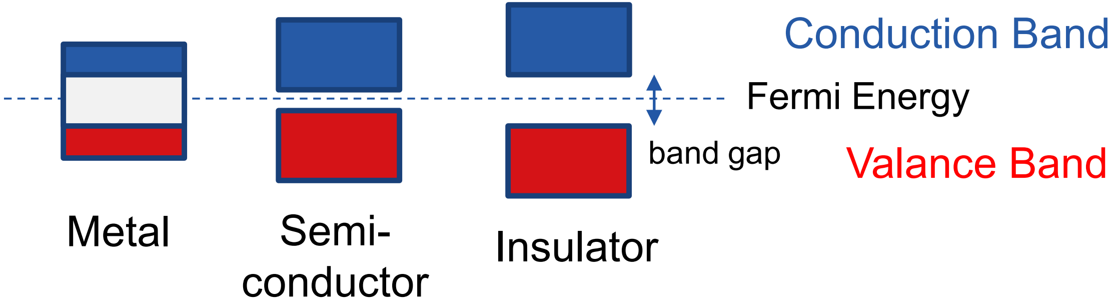
Layout Parasitic Inductance

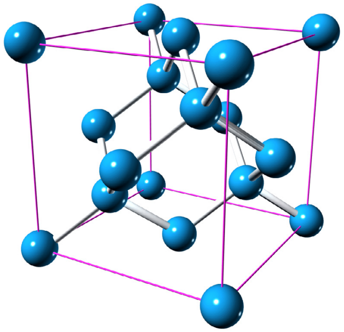
One way of eliminating the influence of layout parasitics is to use isolated gate drivers, isolated power supplies and Kelvin (SS) contacts (note: low side, so functional isolation is sufficient!)



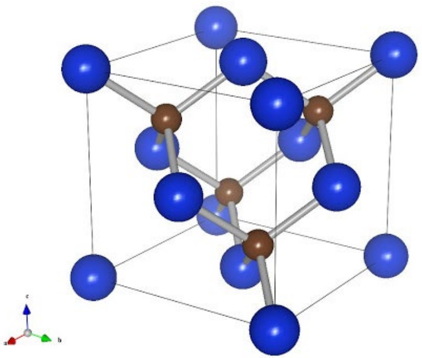
Wide Band Gap Transistors

- Silicon Carbide (SiC)
- Gallium Nitride (GaN)

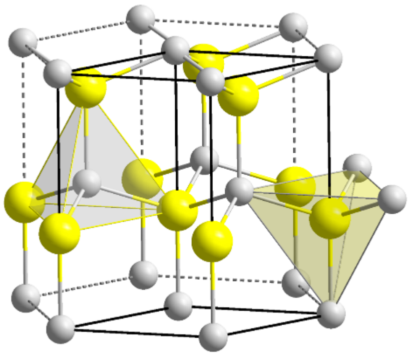




Si



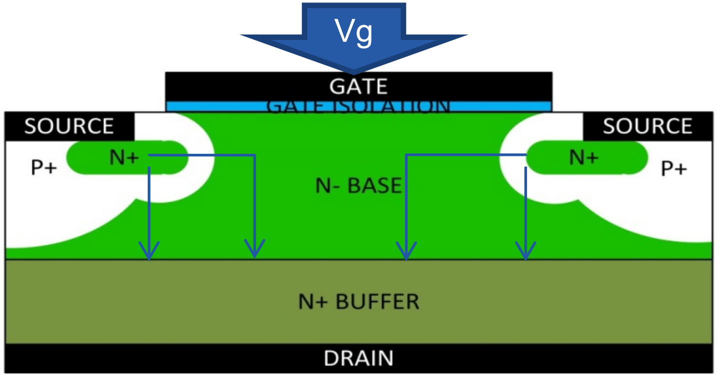
SiC



GaN

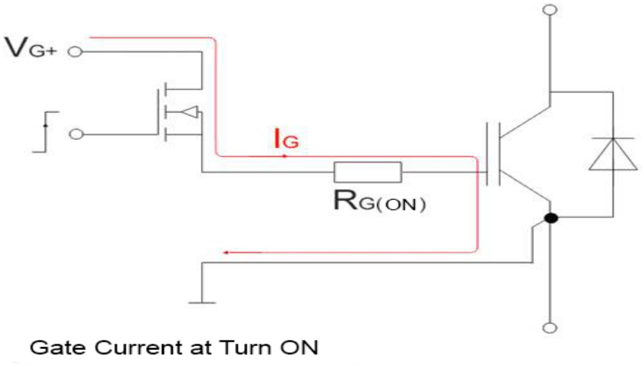
Source: Wikipedia

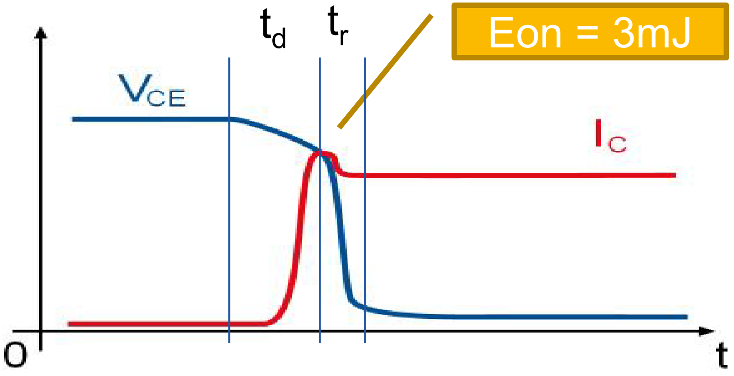
Si/SiC Construction



- SiC 10x higher dielectric breakdown than Si (thinner layers = lower resistance)
- SiC 3x better thermal conductivity as Si (higher power rating)

Turn On Gate Drive: SiC





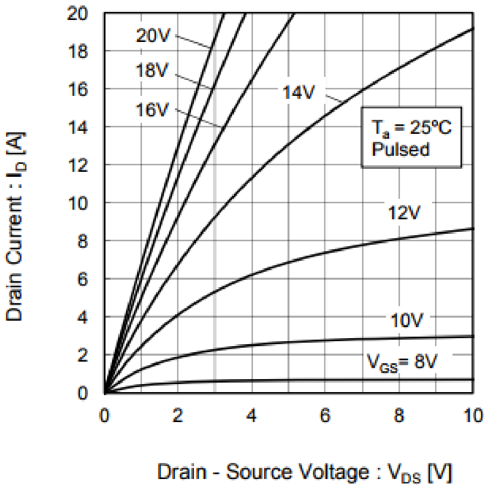
- SiC has significantly lower switching power dissipation than Si
- Switching speed mainly determined by $R_{G(ON)}$ gate resistor

+Ve Turn On Gate Drive: SiC

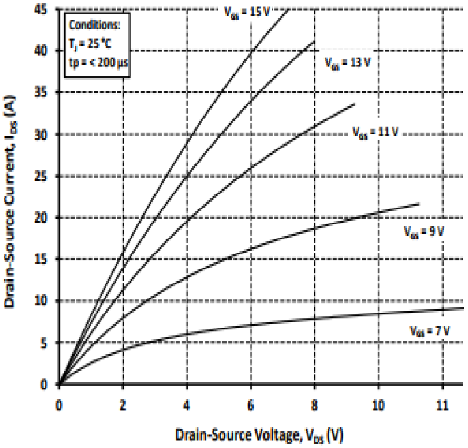
RECOM

+V_{GS} max = +20V (1. Gen)

+V_{GS} max = +15V (2. Gen)



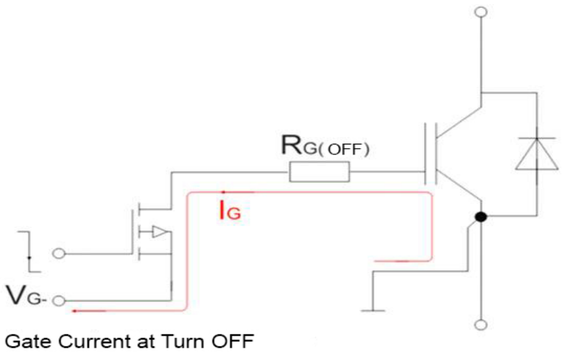
1. Gen

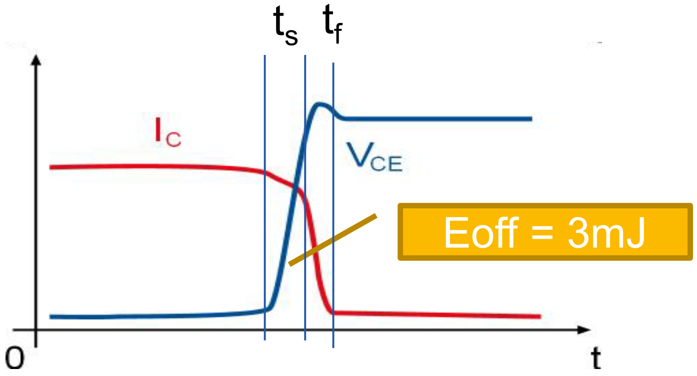


2. Gen

- ≈2V threshold voltage, but 15-20V needed to switch higher currents (fully enhanced)

Turn Off Gate Drive: SiC

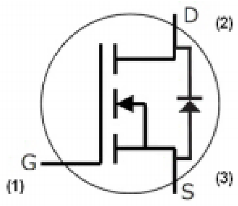




- On and Off switching behaviour very similar (no tail current like IGBT)
- Switching speed mainly determined by $R_{G(OFF)}$ gate resistor

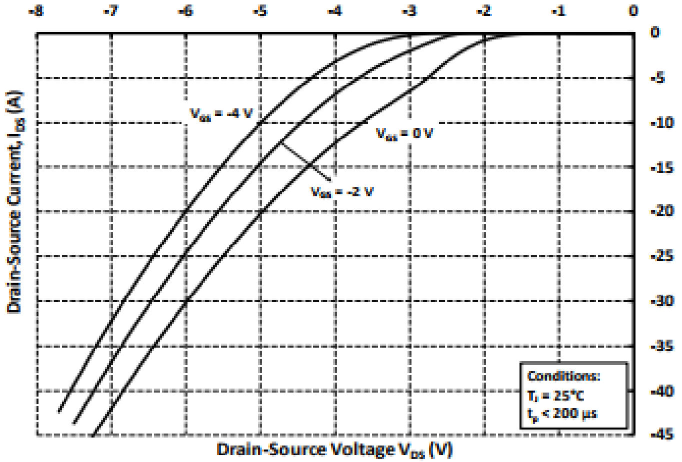
-Ve Turn Off Gate Drive: SiC

$-V_{GS}$ abs. max = -10V (1. Gen)
or -4V (2. Gen)
(limited by the body diode characteristic)

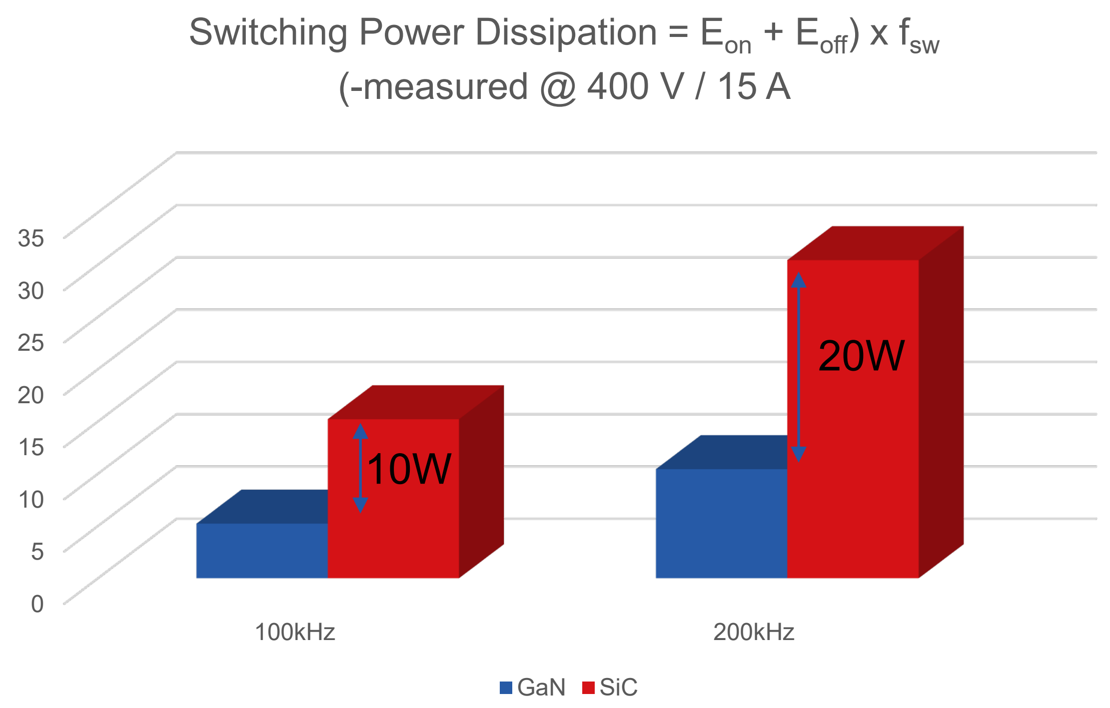


But operation at abs. max.
$-V_{GS}$ reduces the lifetime:

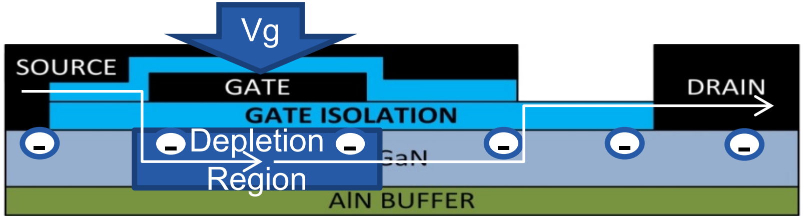
→1. Gen: ideal $-V_{GS}$ = -5V
→2. Gen: ideal $-V_{GS}$ = -3V

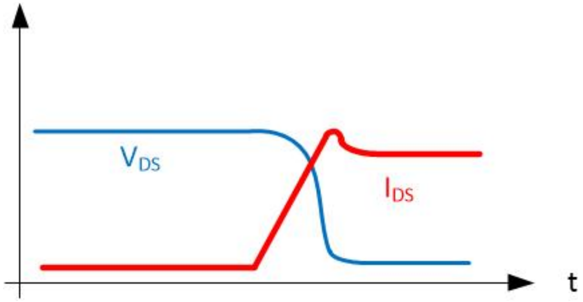


GaN vs SiC-MOSFET



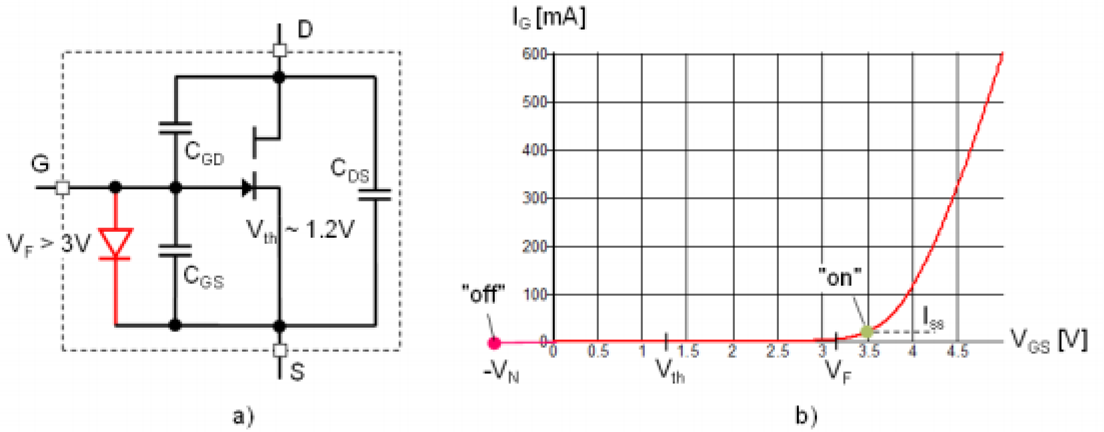
Normally Off GaN E-HEMT





- Significantly lower switching dissipation than Si/SiC (electron injection)
- Inherently bidirectional (no body diode)
- Switching speed mainly determined by R_G gate resistor

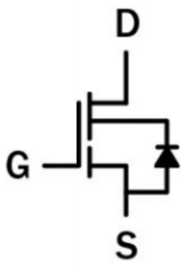
Normally Off GaN E-HEMT

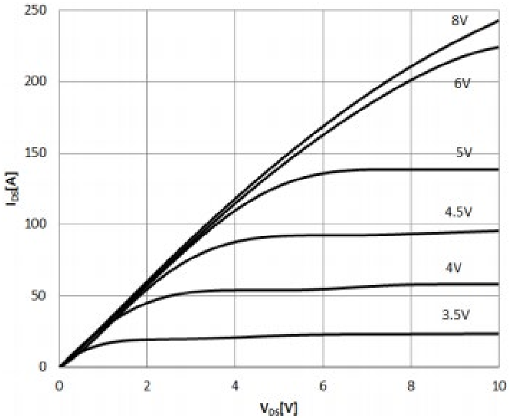


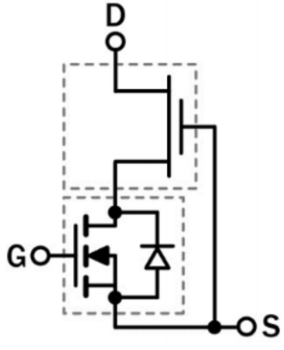
Source: GaN EiceDRIVER™ product family

- Stable V_{TH} (1.2V), but also low abs. max V_{GS}= 6V
- Should be driven with single sided regulated 5V gate driver, or +5/-1V asymmetric gate drive for more gate drive security.

GaN Cascode







- max V_{GS}= ±18V, but no advantage if driven with more than 8V
- Can be driven with single sided 9V gate driver, as a negative gate drive is not needed with the cascode configuration.

Summary so far:

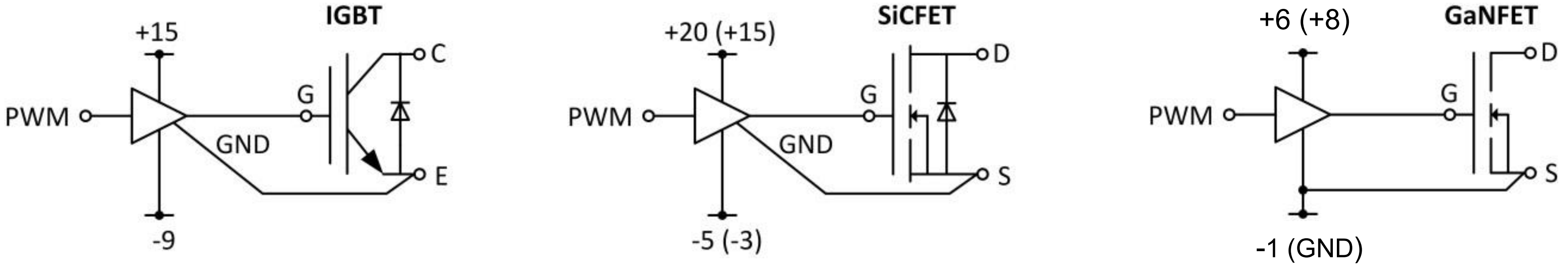
Need to eliminate the influence of parasitics when fast switching:

- Reduce di/dt or dv/dt slew rates (drawback: causes higher losses)
- Balance out L_{Layout} paths (may not be so easy in complex PCBs)
- Use Kelvin contacts to eliminate the effect of ground bounce
- Use negative gate drive (drawback: asymmetric floating supply required)

Summary so far:

Isolated gate drivers:

- Use isolated gate drivers for both high side and low side.
- Different floating output supply voltages are needed depending on type (IGBT, Si-MosFET, 1st./2nd.Gen SiC, E-HEMT GaN, Cascode-GaN)



Reference Design R-Ref01-HB

Half bridge reference design for fast switching (1000VDC)

Suitable for different gate drive voltages, e.g.
+6V, +15V/-3V, +15V/-9V,
+20V/-5V .....

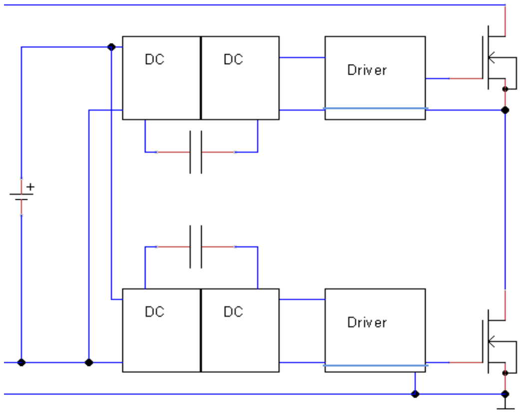
Suitable for TO-247 3-pin and 4-pin transistors

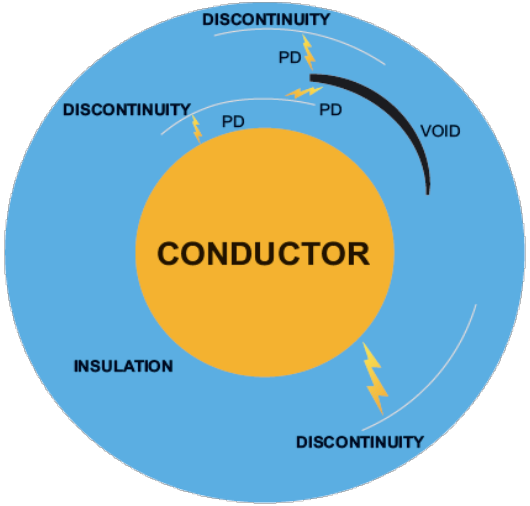
Available at Rutronik

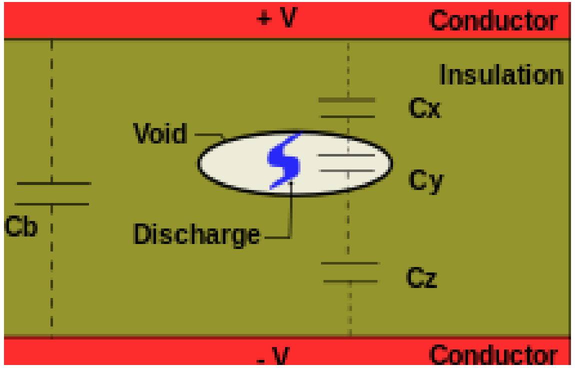
Choosing the Right DC/DC

Why is isolation capacitance so important?

- Partial Discharge







Source: Recom DC/DC Book of Knowledge

Source: Wikipedia

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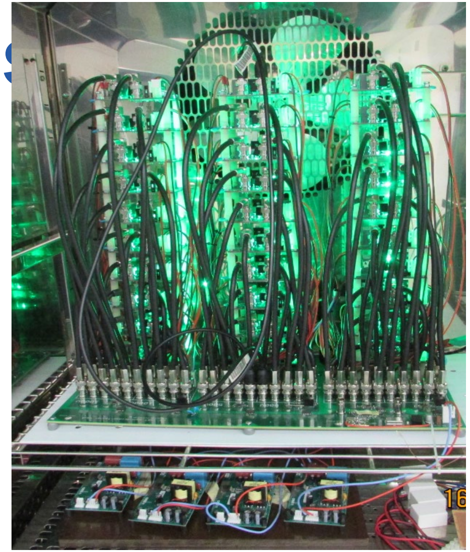
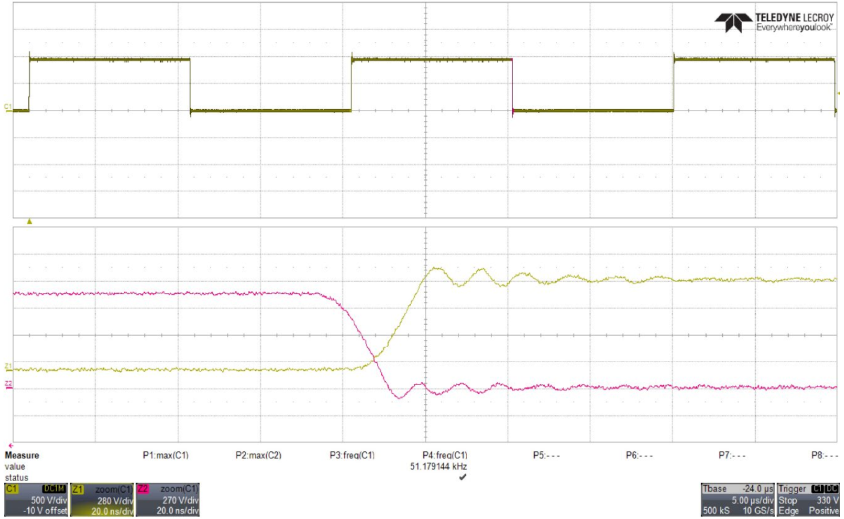
Barrier Insulation Evaluation Res





Recom R&D

Priv.-Doz. Dipl.-Ing. Dr. Techn. Christof Sumereder/TU Graz, FH Johanneum

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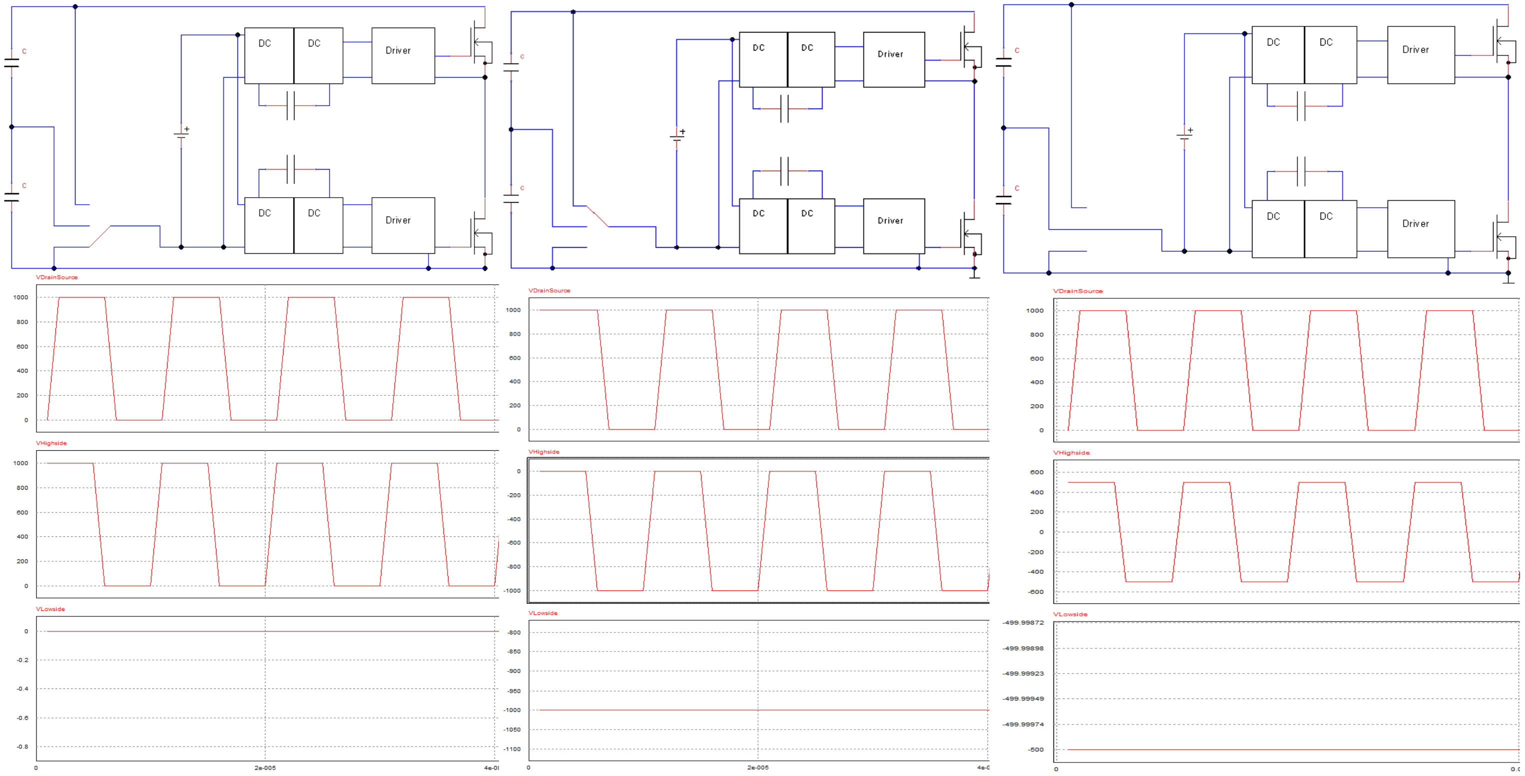
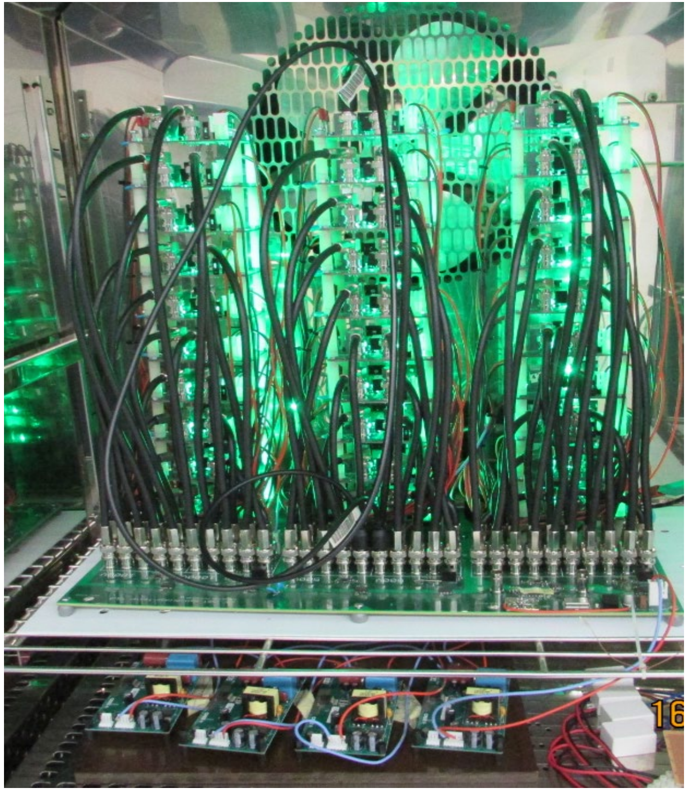


BIER

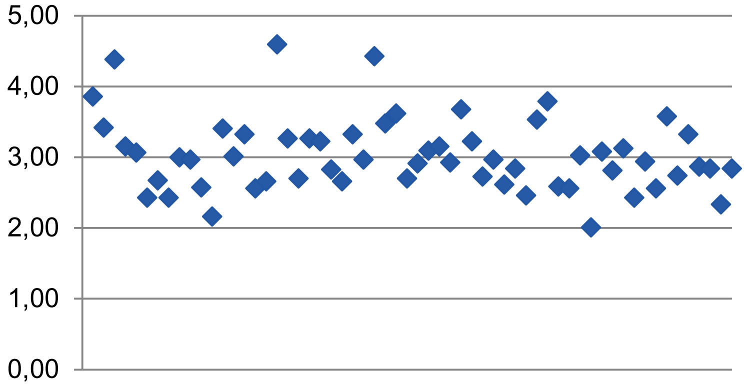
Test Parameters

Test duration:	1464h
Test voltage:	1000V
Ambient temperature:	70°C
DC/DC converter Temp:	93°C
Transistor Temperature	116°C
Switching frequency	50kHz
dv/dt	65kV/µs

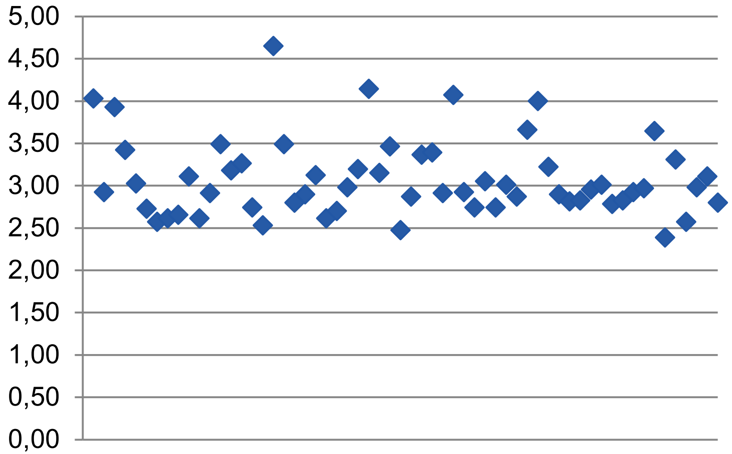


BIER
Partial discharge measurements

VPD Peak [KV] before Test



VPD Peak [kV] after Test



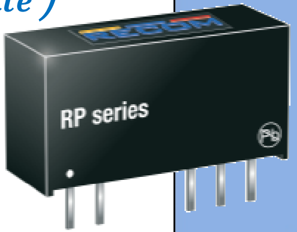
Choosing the Right DC/DC

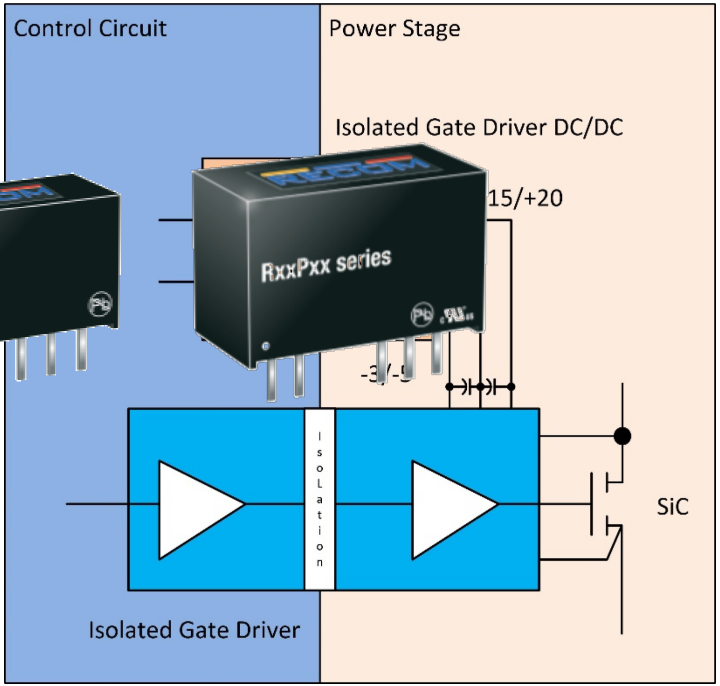
Isolated SiC Gate Driver

$$P_{gate} = P_{driver} + \left(Q_{gate} f_{sw} \Delta_{V_{gate}}\right)$$

$$P_{gate} = 0.05 + 0.25 = 0.3\text{W}$$

(for 50kHz)





Dual Asymmetric output (unreg.)

e.g. **RxxP22005D** (2W, +20V/-5V, 6.4kVDC isolation, 3pF typ, SIP7)

or **RP-1509D** (1W, +15V/-9V, 5.2kVDC isolation, 4pF typ, SIP7)

Choosing the Right DC/DC

Isolated GaN Gate Driver

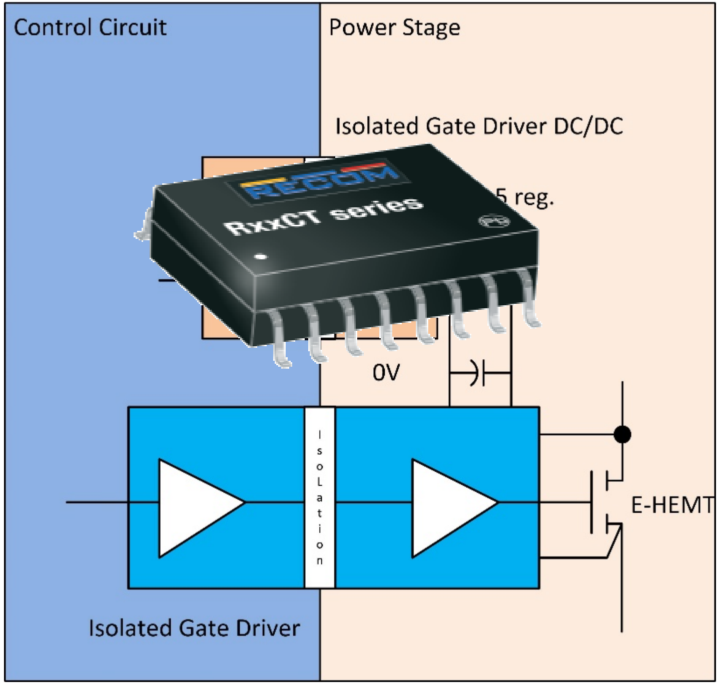
$$P_{gate} = P_{driver} + \left(Q_{gate} f_{sw} \Delta V_{gate}\right)$$

$$P_{gate} = 0.05 + 0.05 = 0.1\text{W}$$

(for 500kHz)

Single Regulated Output

e.g. **R05CT05** (0.4W, +5V reg., 5kVAC reinforced isolation, 3.5pF typ, SOIC-16 SMD)



Choosing the Right DC/DC

R05CT05S

Elektronik Magazine‘s *Product of the Year 2021 Silver Award.*

Choosing the Right DC/DC

Isolated E-HEMT GaN Gate Driver

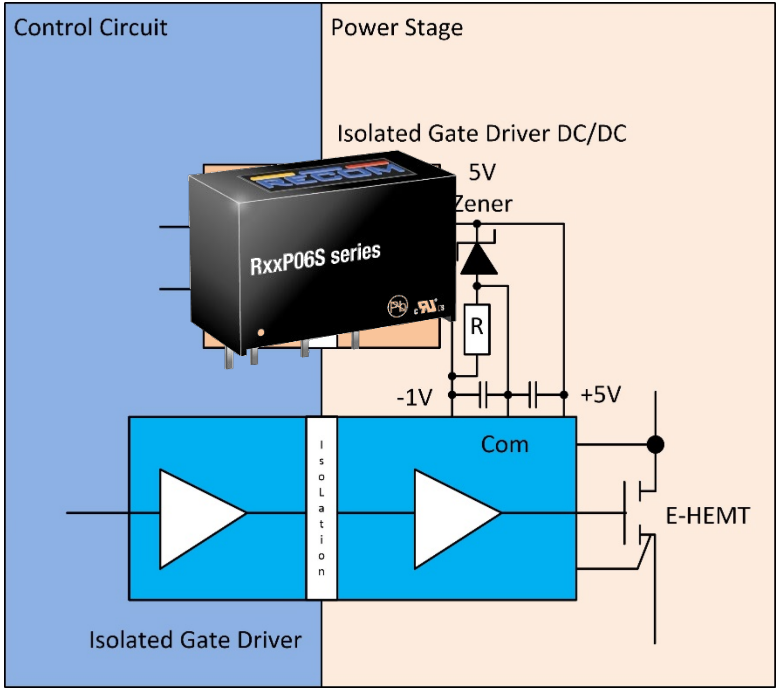
$$P_{gate} = P_{driver} + \left(Q_{gate} f_{sw} \Delta V_{gate}\right)$$

$$P_{gate} = 0.05 + 0.05 = 0.1\text{W}$$

(for 500kHz)

Dual Asymmetric Output (partly regulated)

e.g. **RxxP06S** (1W, +6V, 6.4kVDC isolation, 4pF typ, SIP7)



Choosing the Right DC/DC

Isolated Cascode GaN Gate Driver

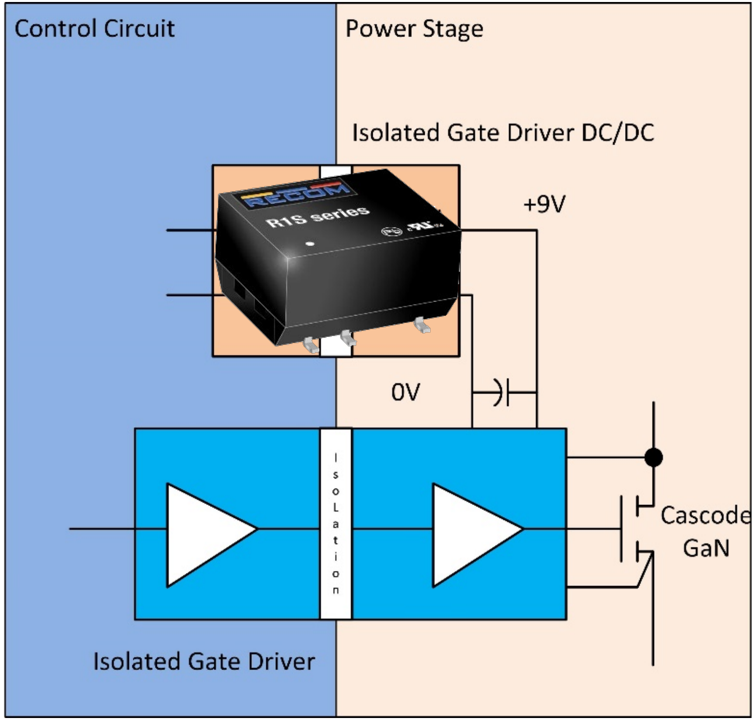
$$P_{gate} = P_{driver} + \left(Q_{gate} f_{sw} \Delta V_{gate}\right)$$

$$P_{gate} = 0.05 + 0.05 = 0.1\text{W}$$

(for 500kHz)

Single Unregulated Output

e.g. **R1S-0509** (1W, +9V, 3kVDC isolation, 15pF typ, 8pin SMD)



Choosing the Right DC/DC

„Solid State Transformer" e.g. stacked 3.3kV/800A SiC power modules

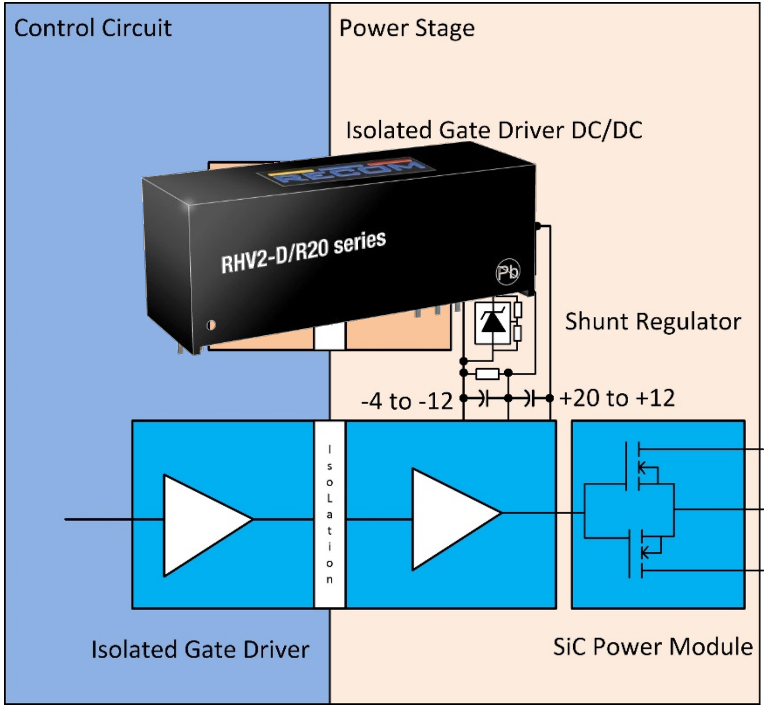
$$P_{gate} = P_{driver+reg} + \left(Q_{gate} f_{sw} \Delta V_{gate}\right)$$

$$P_{gate} = 1.0 + 0.67 = 1.7\text{W}$$

(for 10kHz)

Single Semi-regulated Output

e.g. **RHV2-2424S/R20** (2W, +24V, 20kVDC isolation, 3.5pF typ, SIP16)



Choosing the Right DC/DC

Paralleled Transistor SiC Gate Driver

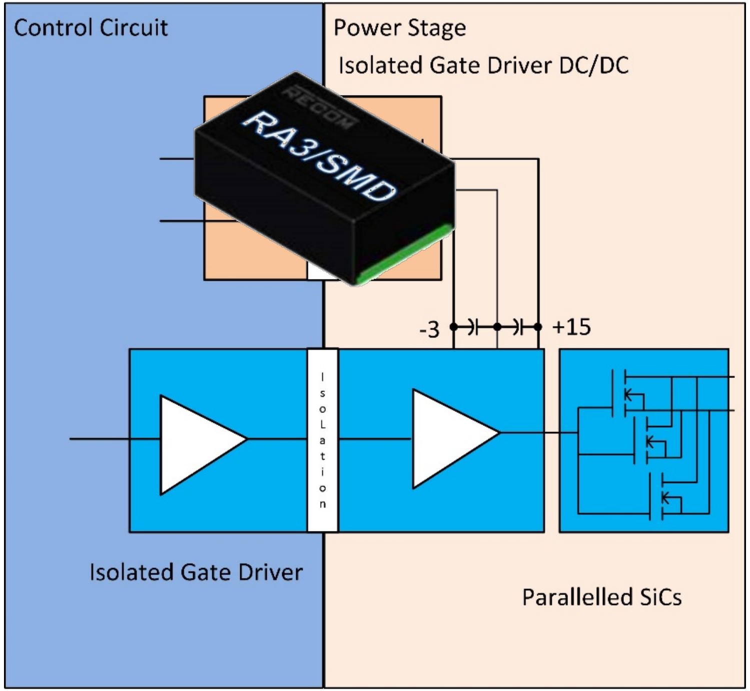
$$P_{gate} = P_{driver} + n\left(Q_{gate} f_{sw} \Delta V_{gate}\right)$$

$$P_{gate} = 0.6 + 3x0.5 = 2.1\text{W}$$

(for 100kHz)

Dual Asymmetrical Outputs

e.g. **RA3-051503D** (3W, +15/-3V, 5.2kVDC isolation, <10pF, Pinless SMD (to be released soon)



High Isolated DC/DC Converters for Gate Drivers

IGBT	SiC	GaN
RxxP2xx, RxxPxx, RP, RH & RKZ series in a compact SIP7 case. RV & RGZ series in DIP14 and DIP24	RxxP21503D, RxxP22005D, RKZ-xx2005D, and RA3 series in compact SIP7 or DIP16 cases	RxxCTxx, RxxPxx, RxxP2xx, RK, RP and RA3 in compact SMD, SIP8 or SIP7 cases
+15V and -9V outputs	+15/-3V and +20/-5V outputs	+5V, +6V, +8, +9V, and +7/-1V outputs
1W or 2W total outputs	2W or 3W total output	1W, 2W, or 3W output power
5V, 12V or 24V inputs	5V, 12V, 15V or 24V inputs	5V, 12V, 15V, or 24V inputs
Up to 86% efficiency	Up to 87% efficiency	Up to 83% efficiency
Symmetric power	Symmetric power or symmetric current output	
Up to 6.4kVDC isolation		
Up to +90°C operating temperature		
EN certified		

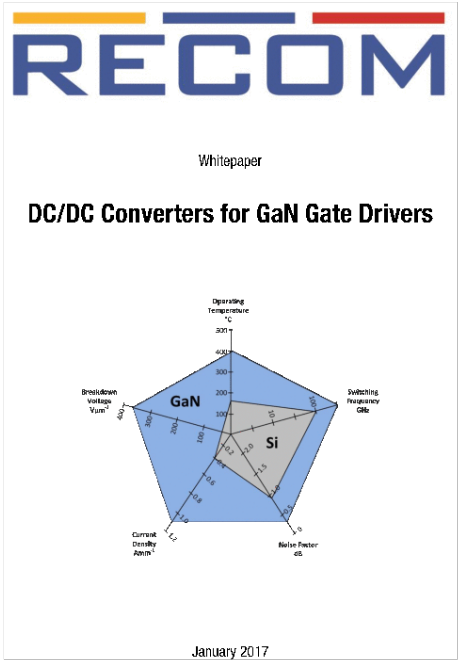
www.recom-power.com/gate-drivers

Summary

RECOM

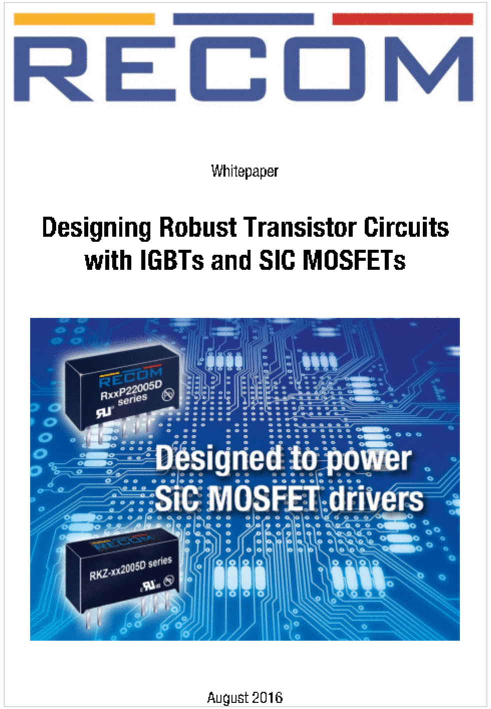
- The voltage on the insulation can be significantly higher than the bus voltage
- High switching speed has an influence on insulation characteristics, so choose high isolation with low isolation capacitance
- Isolation test voltages are often based on low frequencies and may not be representative of true performance.
- Partial discharge measurement gives more information about the insulation than high pot testing
- BIER Test proves : RECOM DC-DC power supplies are suitable for long term high dv/dt without suffering from isolation deterioration.

Website Resources


Whitepaper

DC/DC Converters for GaN Gate Drivers

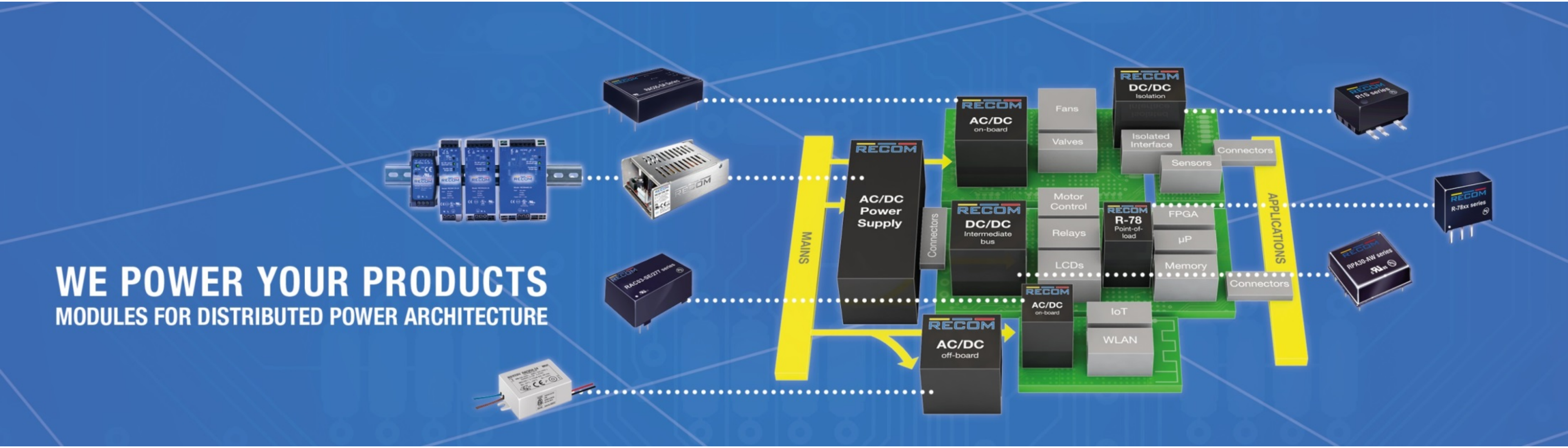
January 2017


Whitepaper

Designing Robust Transistor Circuits with IGBTs and SIC MOSFETs

August 2016

Barrier Insulation Evaluation Research (BIER) Report



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