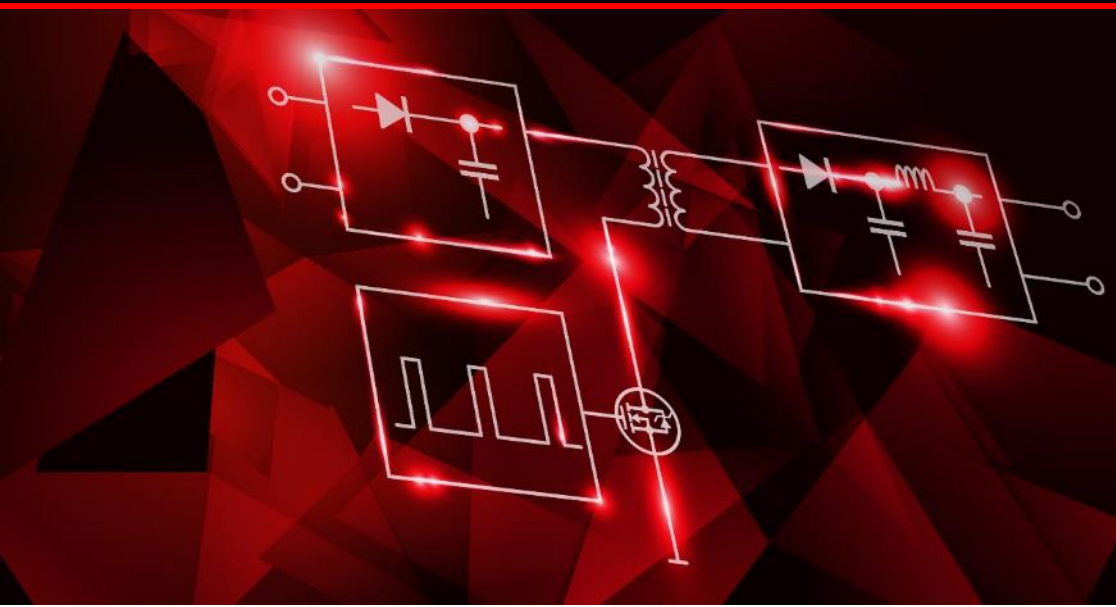
RUTRONIK POWER

RUTRONIK ELECTRONICS WORLDWIDE



RUTRONIK TechTalk meets Gate Driver

Fast switching SMPS Gate Drivers

Ralph Langenberg | Field Application Engineer

Infineon Technologies AG

"Every switch needs a driver !"

High efficiency, high power density and the aim for cost efficient design are todays application requirements.

These are in turn requiring fast switching, short dead times and low losses while keeping normative like safe isolation and interference immunity.

Infineon helps you selecting the relevant features in a gate drivers datasheet, which aspects to cover in your design and layout and how to address EMI topics.

Infineon Technologies AG

Agenda

- Output current
- Low ohmic output stages
- Buffer caps
- Timing
- UVLO
- Fast active clamping
- Layout considerations
- Portfolio overview and selection tools

Some suitable applications

Solar, UPS, Battery Management

- UPS up to 10 kvA
- Solar inverter
- Medium voltage battery management systems

Telecom – non-isolated DCDC

- Basestation marco and distributed

Battery Powered Applications

- Power tools
- Light electric vehicles
- Service robots

Server & storage

- Server–Intel/IBM/AMD/ARM
- Workstation
- Storage
- Artificial intelligence

SyncRec for SMPS HP+LP

- Telecom and server PSUs
- Adapter and charger

Telecom – isolated DCDC

- Brick converters
- Protection ICs

Class-D Audio

- High-End audio systems
- Battery powered speakers
- Smart speakers

WLS Charging

- Qi WLS charging solutions
- A4WP wireless charging solutions

High-end consumer

- HE desktop/notebook
- Gaming
- Graphic
- Industrial PC

Relevant parameter in the Gate-driver's Datasheet:

- Number of channels
- Isolation or level-shifter
- Output current
- Voltage class
- Package

- something else… ?

EiceDRIVER™ 1EDBx275F

Single-channel isolated gate-driver ICs in 150 mil DSO package

Description

EiceDRIVER™ 1EDBx275F is a family of single-channel isolated gate-driver ICs, designed to drive Si, SiC and GaN power switches.

1EDBx275F is available in an 8-pin DSO package with 4 mm input-to-output creepage distance; it provides isolation by means of on-chip coreless transformer (CT) technology.

With tight timing specifications, 1EDBx275F is designed for fast-switching medium-to-high power systems. Excellent common-mode rejection, low part-to-part skew, fast signal propagation and small package size make 1EDBx275F a superior alternative to high-side driving solutions using optocouplers or pulse transformers.

Features

- Single-channel isolated gate-driver
- 45 ns input-to-output propagation delay with excellent accuracy (+4/-4 ns)
- Separate low impedance source and sink outputs
- Fast clamping of parasitics-induced output overshoots under UVLO conditions
- Fast start-up times and fast recovery after supply glitches
- Optimized UVLO levels (4 V, 8 V, 13 V) for Si, SiC and GaN transistors
- High common mode transient immunity (CMTI > 300 V/ns)
- Available in 8-pin 150mil DSO package
- Qualified for industrial grade applications

Isolation and safety certificates

- UL1577 with V_{ISO} = 3000 V_{RMS} (certification pending)

Potential Applications

- Server, telecom and industrial Switch-Mode Power Supplies (SMPS)
- EV power modules, motor drives and power tools
- Solar power inverters and Uninterruptable Power Supplies (UPS)

Table 1 EiceDRIVER™ 1EDBx275F Portfolio

Part number	Peak source / sink current	UVLO ON / OFF	Isolation certification	Package
1EDB7275F	5.4 A / 9.8 A (for V_{DDO} = 15V)	4.2 V / 3.9 V	UL1577 (V_{ISO} = 3000 V_{RMS})	PG-DSO-8
1EDB8275F		8.0 V / 7.0 V		
1EDB9275F		13.7 V / 12.9 V		

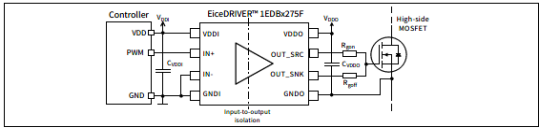


Figure 1 Typical application

Final Data Sheet
www.infineon.com
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Rev. 2.0
2020-04-08

Fast switching SMPS Gate Drivers

- Relevant parameter in the Gate-driver's Datasheet:
  - Output current: what does a certain peak value mean in the application
  - Timing: propagation delay, pd mismatch pulse width min, distortion dead-time
  - UVLO: threshold and timing
  - Clamping: startup behavior
- Design considerations
- Layout considerations

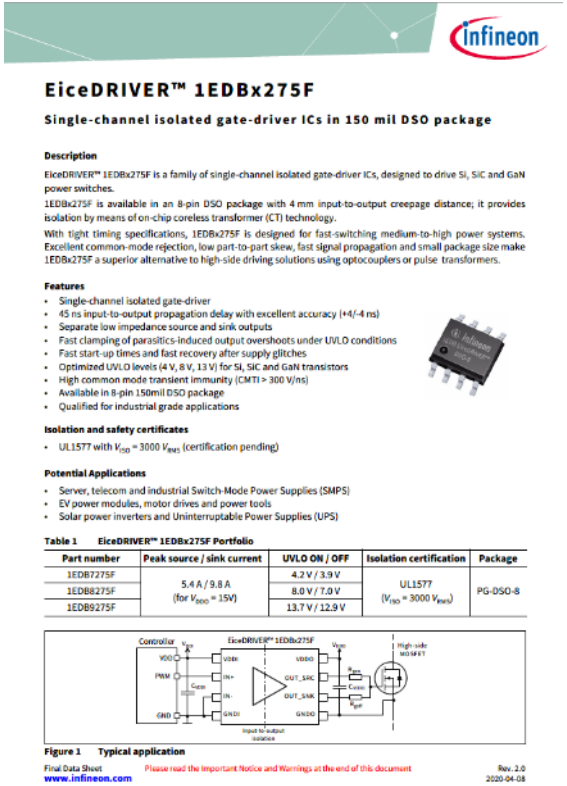

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Figure 1 Typical application

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Output Current

Gate-driver Datasheets – Output current

- Investigate the output capability of
  Infineon isolated products vs. Competitors

- In this investigation
  - 1EDC60I12AH (typ. I_{OH} = 10 A)
  - 1ED3124Mx12H (typ. I_{OH} = 14 A)
  - Competitor U (configured as unipolar) (typ. I_{OH} = 17 A)

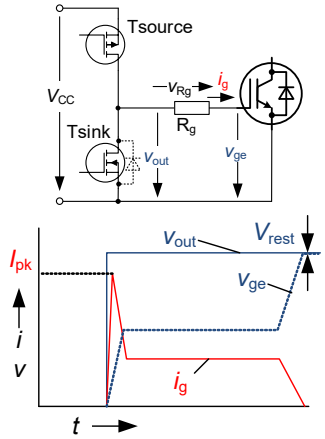
- Lets investigate switching behavior of the devices and their capabilities
  - with capacitive load
  - with an IGBT7 module (**FF900R12ME7_B11**)

  Observe the strengths and weaknesses of each product

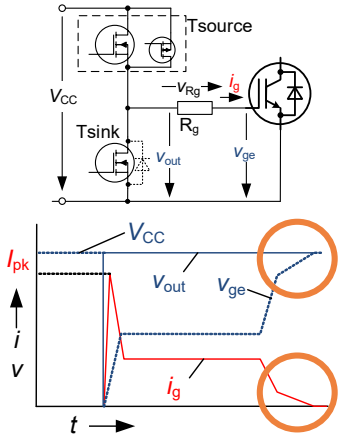
Comparison of selected output section topologies?

P-channel N-channel



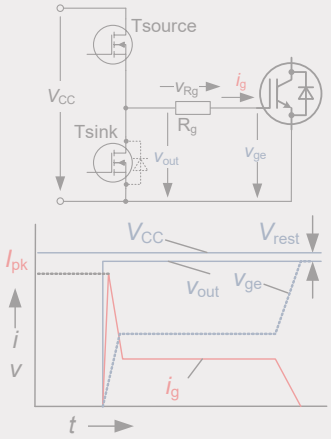
- Strong on-current@Miller
- Rail2Rail

(P+N)-channel N-channel



- High $R_{DS(on)}$ p-channel can bring more losses
- Weak on-current@Miller
- Rail2Rail

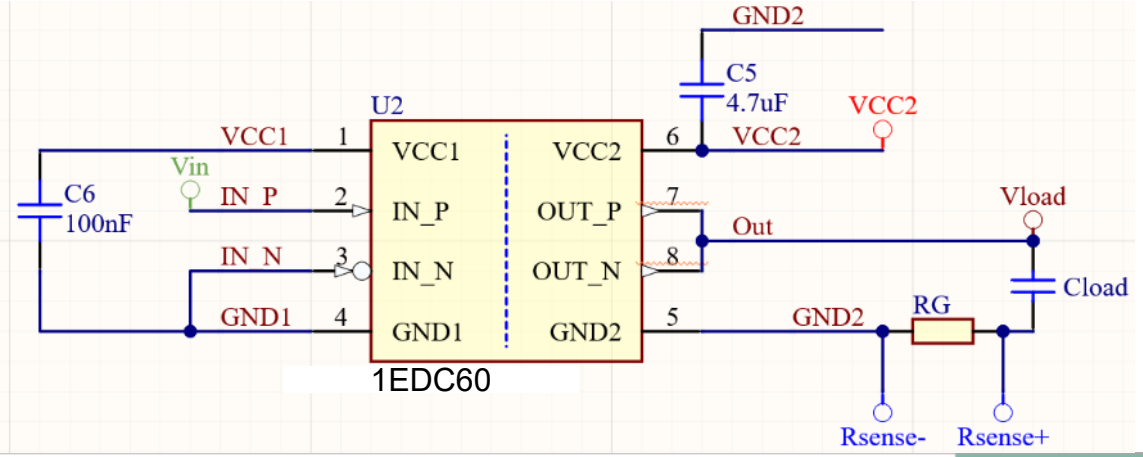
N-channel N-channel



- Voltage remainder for on-state (no rail2rail)
- Needs over-drive -> bad effects and work-arounds

Capacitive load turn-on – sample test setup

- The gate loop was kept low inductive
- Capacitive load: C_{load} = 220nF
- R_g (also used for current measurement) =
  - 0.05 Ω (to observe the unimpeded gate driver behavior)
  - 1.00 Ω (at the lower limit of the range where such gate drivers are fully exploited)
  - 10.0 Ω (quite large value for such gate drivers, at the upper feasibility limit)
- V_{VCC2} = increasing from 15V to 24V, in 1 V steps
- T_j =25°C & 85°C

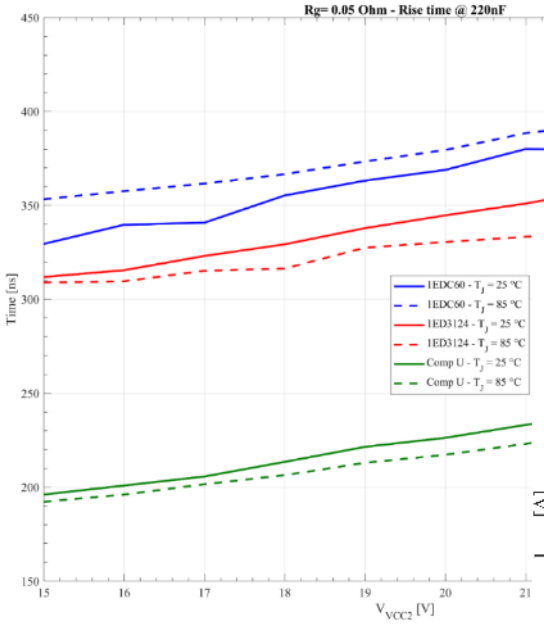


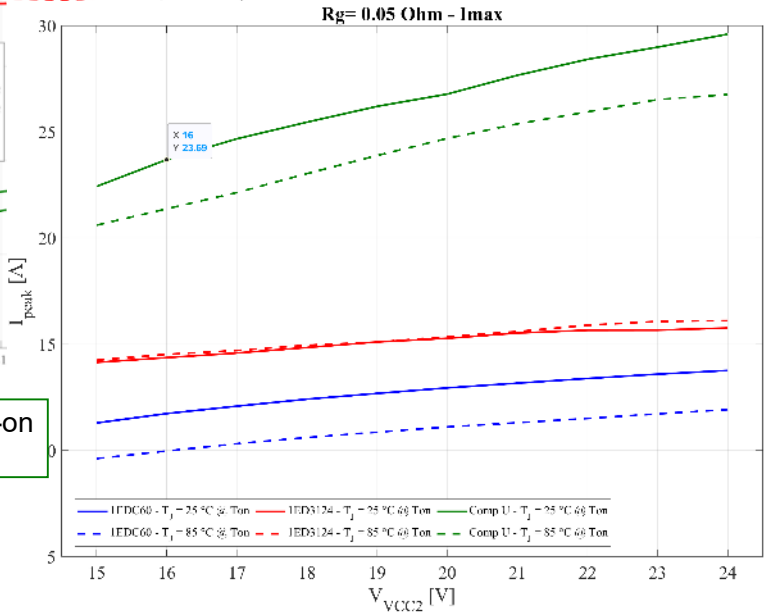
Capacitive load – Rise time & Imax – Rg = **0.05 Ohm**

- Rise time (10% ↑ 90%)
- Peak output current
  (w/o inductive overshoots)
  - Blu: 1EDC60
  - Red: 1ED3124
  - Grn: Comp.
  - Solid: 25°C ——
  - Dashed: 85°C ----

- C_{load} = 220nF

- Competitor: bootstrap circuit may boost the n-channel performance at turn-on for a short time

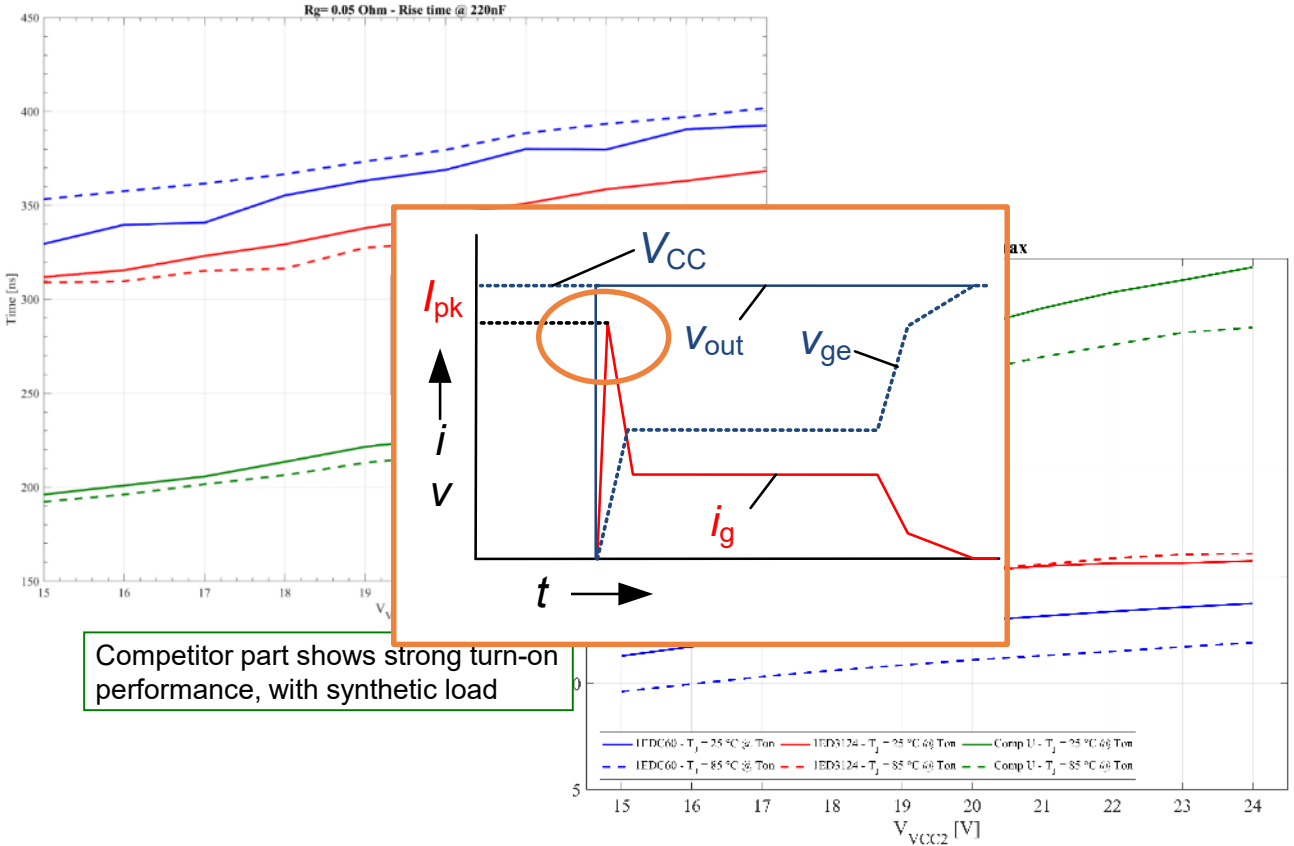




Competitor part shows strong turn-on performance, with synthetic load

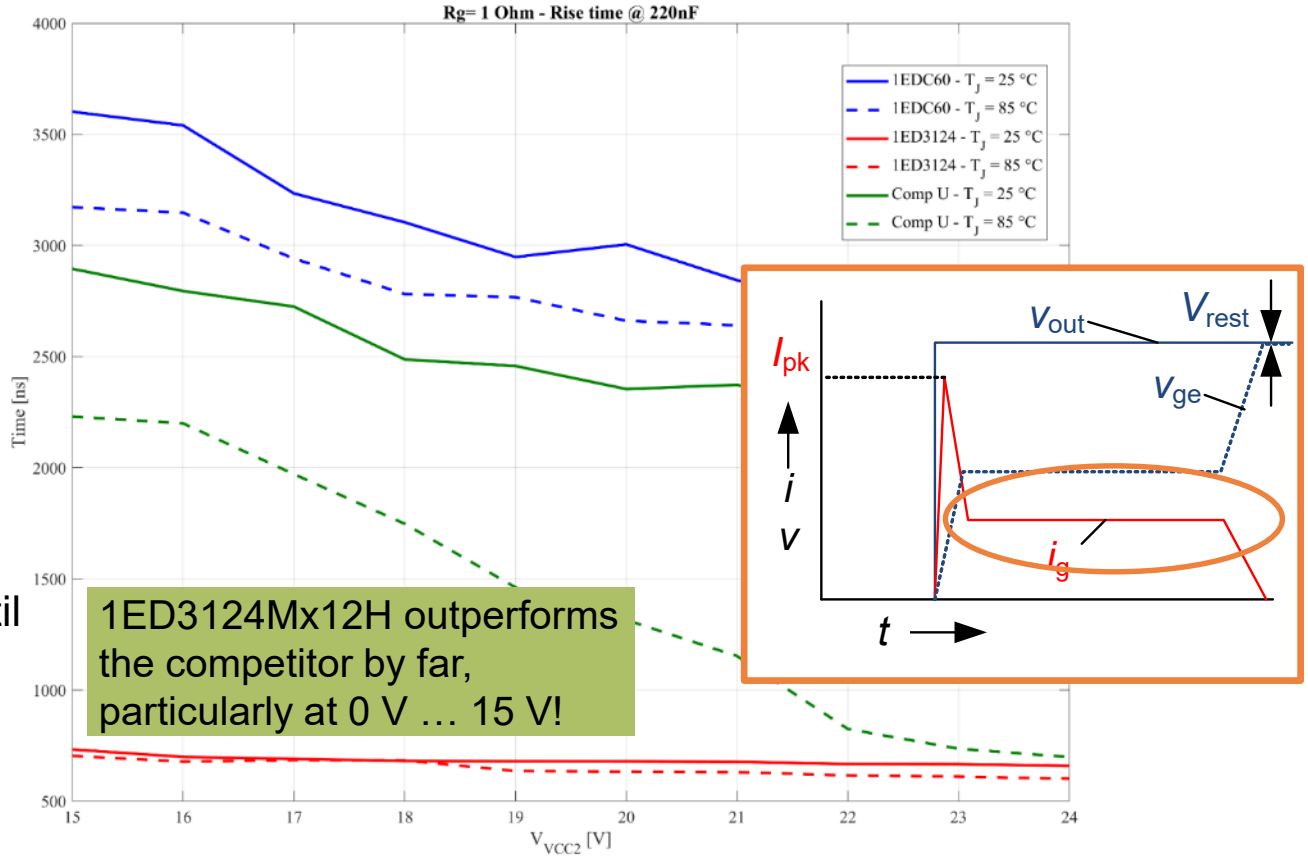
Capacitive load – Rise time & Imax – Rg = **0.05 Ohm**

- Rise time (10% ↑ 90%)
- Peak output current
  (w/o inductive overshoots)
  - Blu: 1EDC60
  - Red: 1ED3124
  - Grn: Comp.
  - Solid: 25°C ——
  - Dashed: 85°C ----
- C_{load} = 220nF
- Competitor: bootstrap circuit may boost the n-channel performance at turn-on for a short time



Capacitive load – Rise-time – Rg = **1 Ohm**

- Rise time (10% ↑ 90%)
  - Blu: 1EDC60
  - Red: 1ED3124
  - Grn: Comp.
  - Solid: 25°C ——
  - Dashed: 85°C ----
- C_{load} = 220nF
- The strong p-channel of 1ED3124MC12H can deliver turn-on current until the end!

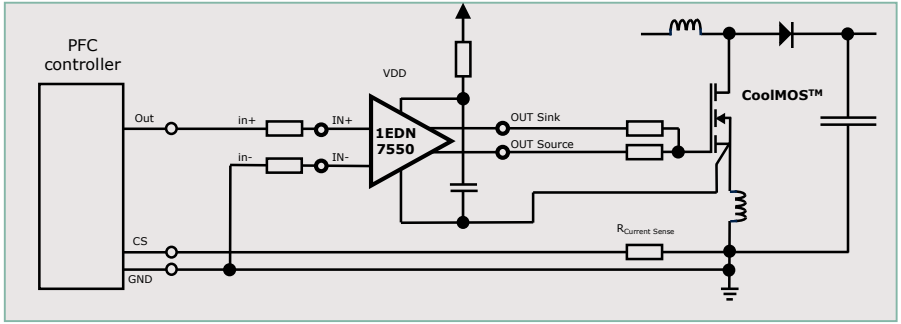


Lower Losses
due to low-ohmic output stages

Taking advantage of true rail-to-rail low-ohmic output stages: example: 1EDN7550 (special hint → TDI: true-differential input)

Compatible

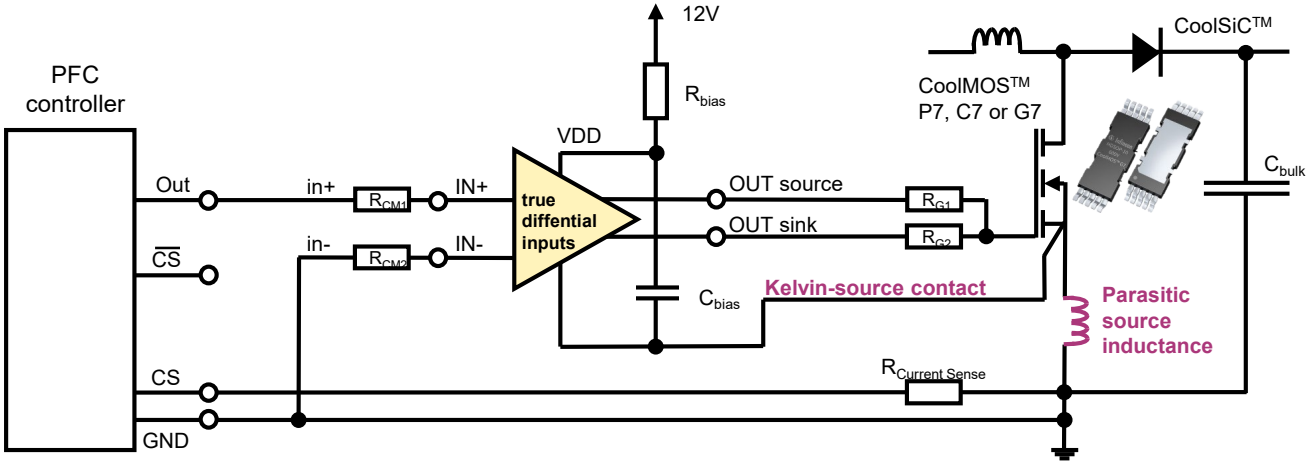
- Packages: DSO TSSOP WSON
- Power: 2x +/-5A
- Pace: 19 ns propagation delay
- Precision: 1 ns channel-to-channel Propagation Delay Matching
- Price: Competitive



Better

- Truly low-ohmic output stages:
  - Least internal power dissipation
  - More effective gate-drive power
  - 0.65 Ω **P-FET** / 0.5 Ω N-FET
- -10 V Input robustness:
  - Crucial noise margin
  - to safely drive pulse transformers
- 5 A reverse current robustness
  - No need for Schottky clamping diodes
  - Higher power density, lower BoM
- 8V UVLO Protection:
  - Fast and reliable SuperJunction and
  - Standard-Level MOSFET protection

Quick intro: Driving the MOSFETs with True Differential Inputs

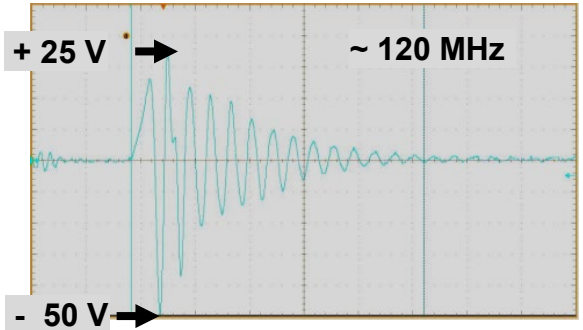


GND-shift:

PFC controller

vs.

Gate driver IC

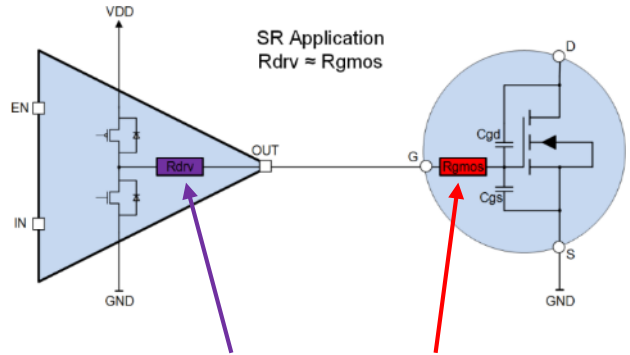


Gate driver with differential inputs:

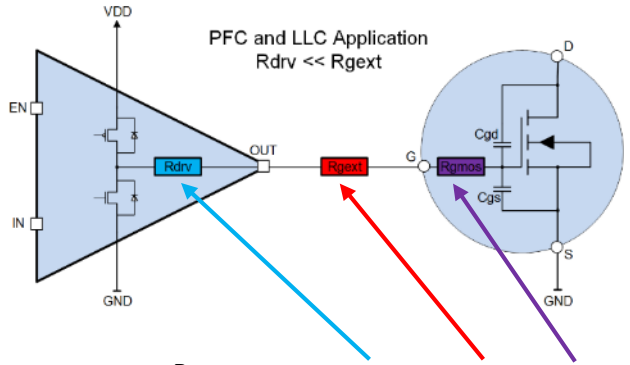
- Robust against +/-150 V AC_{pk} GND-shifts
- Small SOT-23
  Tiny TSNP-6

Low Rdson output stage extends application coverage

The theory behind: How is the driving power distributed



$$P_{total} = \frac{P_{total}}{R_{drv}+R_{gmos}} \left(R_{drv} + R_{gmos} \right)$$

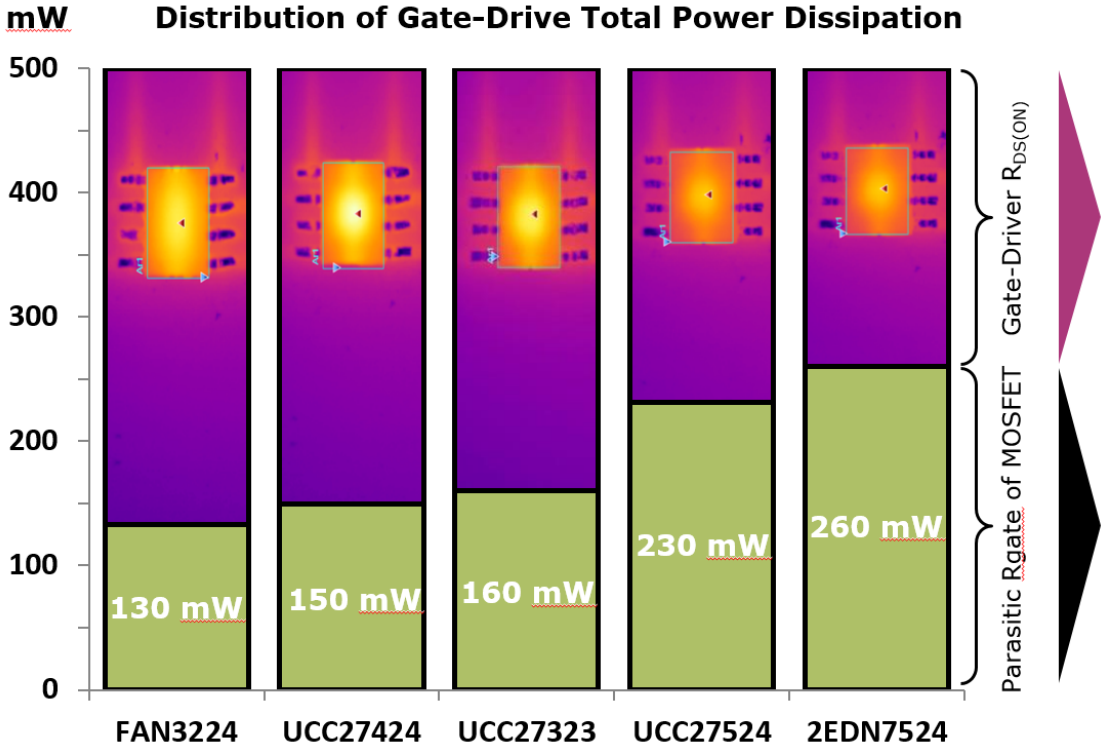


$$P_{total} = \frac{P_{total}}{R_{drv}+R_{gext}+R_{gmos}} \left(R_{drv} + R_{gext} + R_{gmos} \right)$$

$$P_{total} = C_{g\_tot} * V_{DD}{}^2 * f_{SW} = Q_{g\_tot} * V_{DD} * f_{SW}$$

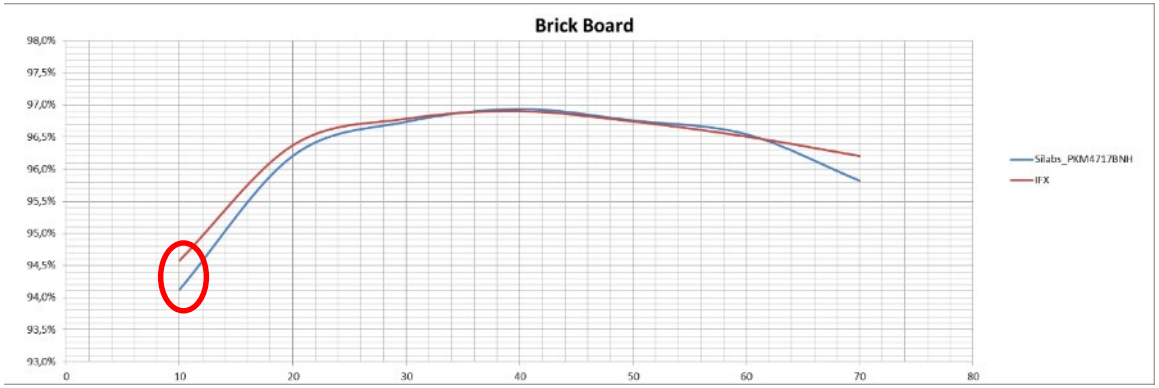
C_{g_tot} = Total Gate Capacitance
Q_{g_tot} = Total Gate Charge
V_{DD} = Driver Supply Voltage
f_{SW} = Switching Frequency

Taking advantage of true rail-to-rail low-ohmic output stages: 1EDN up to 2x more effective gate-drive power



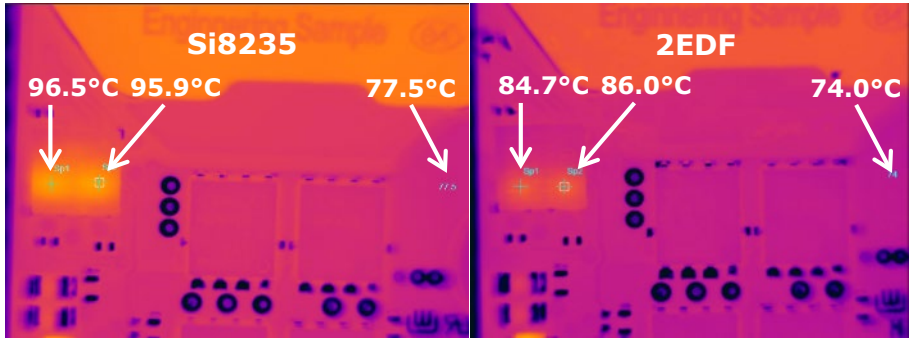
Use-Case: Synchronous Rectification with 50% duty-cycle, 250 kHz
2x 3 OptiMOS™ 1mOhm 30V in parallel, 2-layer JEDEC 51-7 PCB

Driver P_D comparison on 750W 1/4Brick: IFX 2EDF vs. Silabs Si8235



Cooler Driver Advantages:

- Flexibility in thermal design
- Can drive faster/more FETs within thermal budget
- Better reliability



Use-Case:

- Sync. Rectification
- 2x 2 OptiMOS BSC010NE2LSI 1mΩ / 25V in parallel,
- 0.5Ω / 12nF RC load equivalent
- fs=200kHz,
- Vgs=8V

Gate-driver Datasheets – Output current – conclusions

- Datasheet-test-conditions can be misleading
  - Synthetic tests, as used for datasheets with unrealistically small capacitors, can be misleading and some competitors might appear better.

- Gate driver ICs do only show their realistic behavior when paired with a power transistor.

- It is most important to select gate drivers having a strong p-channel FET for turn-on, such as the X3-Comapct family.

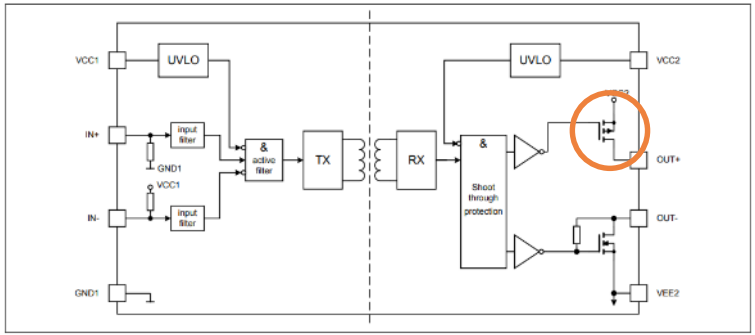
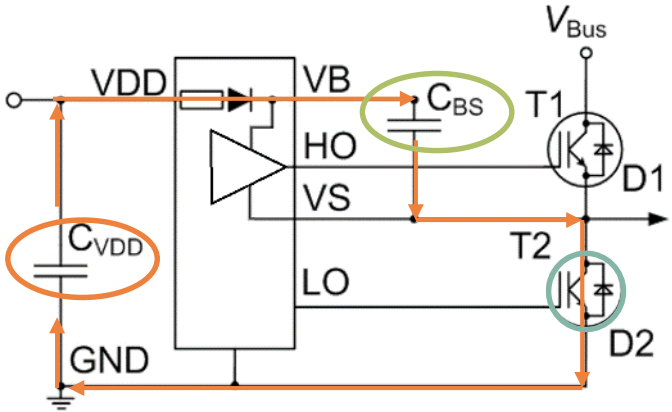


Figure 2 **Block diagram separate source and sink output variants**

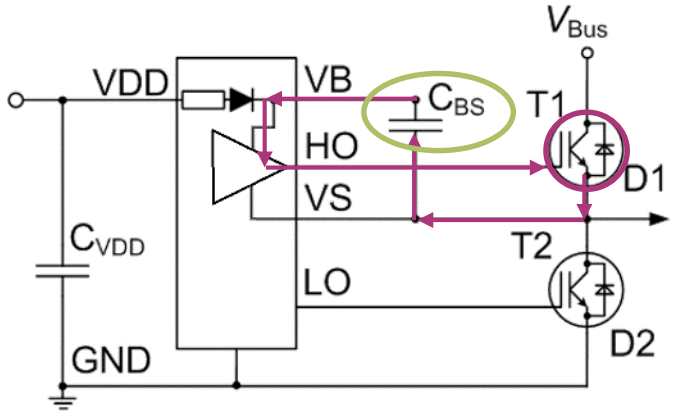
Buffer Caps

Understanding the importance of by-pass capacitor C_{BS}

- C_{BS} charges *only* during LowSide-FET ON-time
- Energy transfer between caps C_{VDD} and C_{BS} - not from supply !
  - Requires low ESR caps and low impedance connections.



- C_{BS} supplies gate current during HighSide-FET ON-time
- Energy transfer between caps C_{GD} and C_{BS}!



Bypass capacitor: Comparison of different C_{BS} values

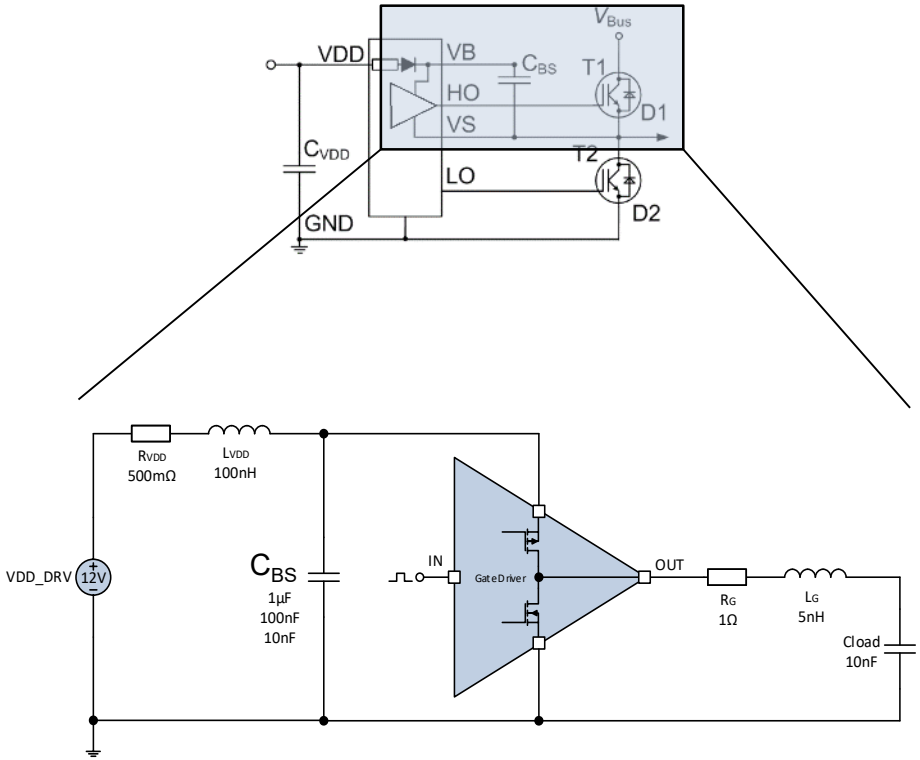
- Driver supply system in more detail
  - C_{BS} charges C_{load}(*)
  - V_{CBS} drops
    - (beware of UVLO, V_G !)
    - $\Delta Vdd_{drv} = Vdd_{drv} * \frac{C_{load}}{C_{BS}}$
  - If we require:

$$\Delta Vdd_{drv} = 5\%$$

  - We need:

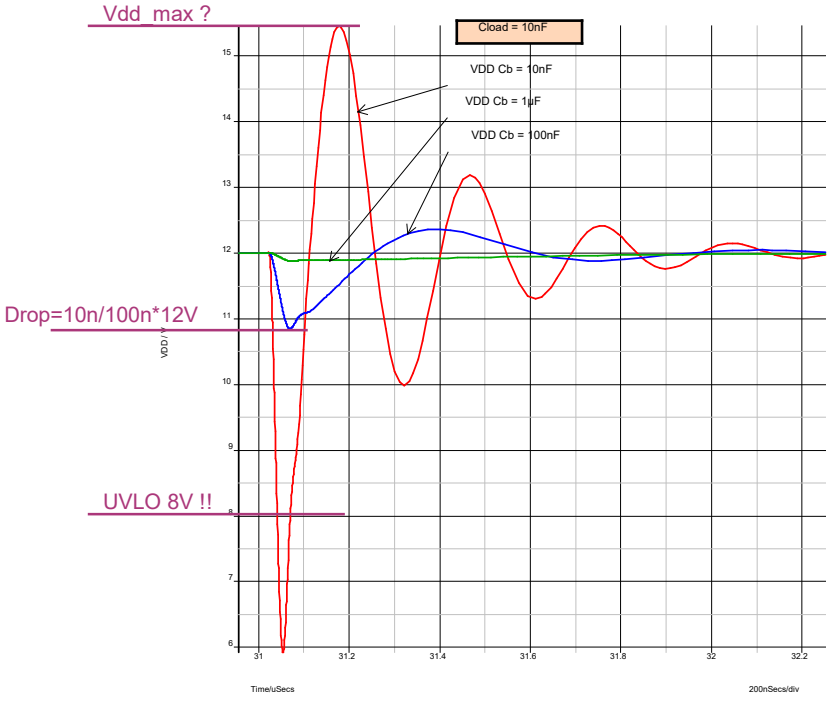
$$C_{BS} = 20 * C_{load}$$

(*) $C_{load} = \frac{QG}{V_{GS}}$

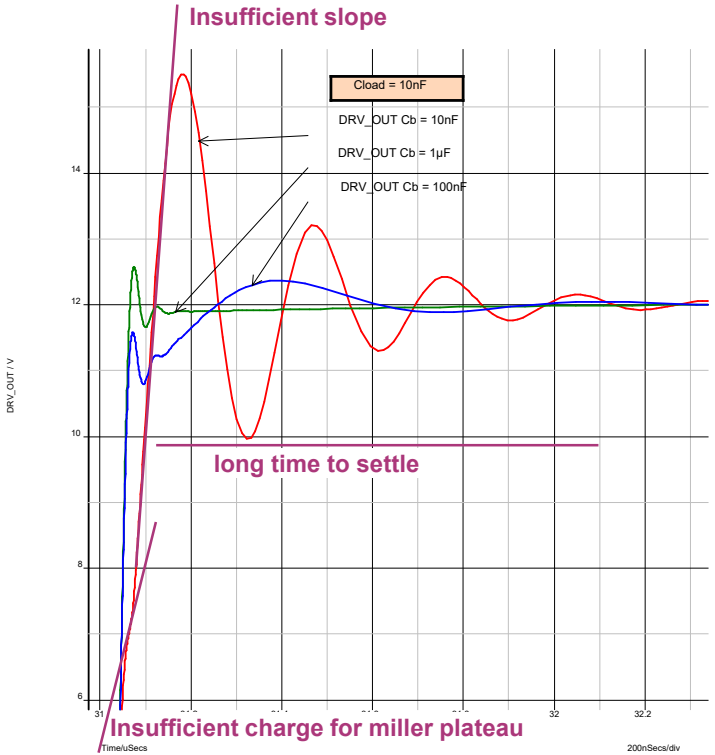


Bypass capacitor: Comparison of different C_{BS} values

Simulation driver supply voltage



Simulation driver output voltage

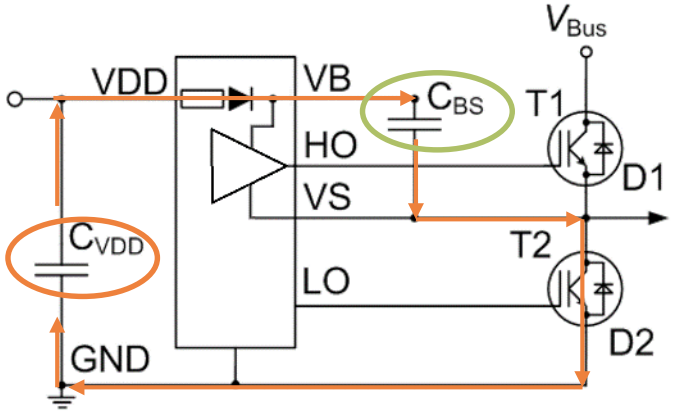


Bypass capacitor at the supply side: C_{VDD}

- Same applies for relation C_{VDD}/C_{BS}
  - Select low ESR,

    $C_{VDD} \geq 20 \bullet C_{BS}$

  - Place C_{VDD} close to Vdd-pin
  - Avoid leakage inductance in the path from supply to C_{VDD} to avoid ringing.



Timing

How does precision timing help ?

- Short and precise dead-times lead to more efficient designs.
  - During dead time no energy is transferred.
  - Too short DT leads to risk of shoot-through

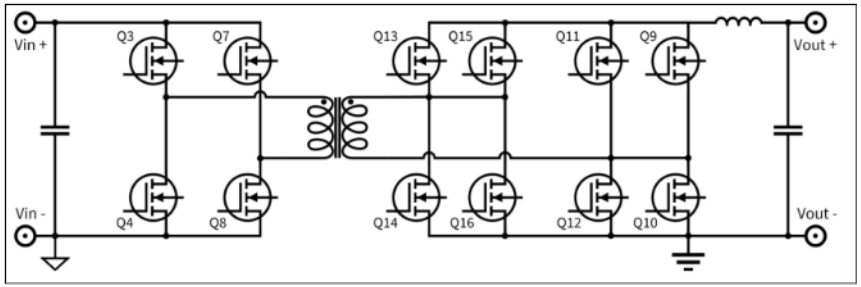
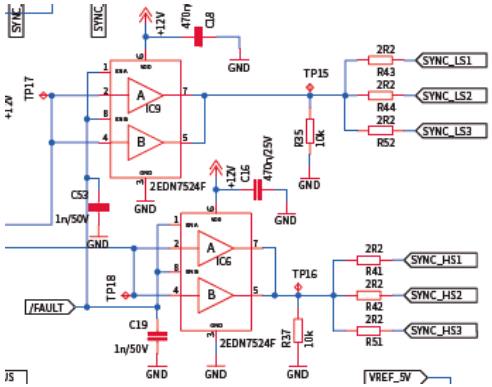
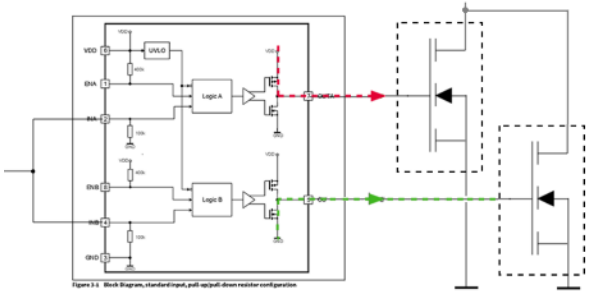


Figure 2 **Topology of the FB-FB rectifier**

- Precise timing enables
  - paralleling of PowerFETs
  - paralleling of Drivers





1EDB Family cross-reference

All in 150mil 8-pin DSO package and with same pinout

- All Infineon 1-channel galvanically isolated gate-driver ICs can be found at: https://www.infineon.com/cms/en/product/power/gate-driver-ics/high-side-drivers/

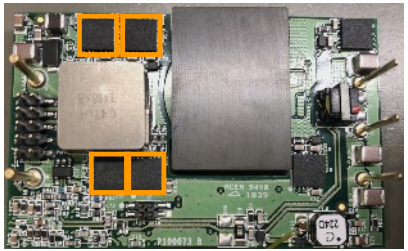
	Part number	Isolation		Typ. V_{DDO} UVLO		Max. V_{DD}	Typ. Input Filter Time [ns]	Typ . Propagation Delay [ns]	Propagation delay accuracy over temperature & production	Typ. output current (V_{DDO} = 15V, V_{out} = 0 V, @ RT		data sheet
		Certification	Rating	turn on	turn off					Source	Sink	
Infineon	1EDB6275F	UL1577 (pend.)	V_{ISO} = 3000 V_{rms}	12.2 V	11.5 V	20 V	19 ns	45 ns	+/- 4 ns	5.4 A_{peak}	-9.8 A_{peak}	3.8.20, Rev. 2.1
	1EDB7275F			4.2 V	3.9 V							
	1EDB8275F			8.0 V	7.0 V							
	1EDB9275F New			14.9 V	14.4 V							
Infineon	1EDI20N12AF	n.a.	V_{ISO} = ± 1200 V_{DC}	9.1 V	8.5 V	35 V	40 ns	115 ns (on) 120 ns (off)	+ 23 / - 25 ns @ 25°C	4 A_{peak} 10 A_{peak}	-3.5 A_{peak} -9.4 A_{peak}	1.6.15, Rev. 2.0
	1EDI60N12AF											
	1ED3124MU12F New	UL 1577	V_{ISO} = 3000 V_{rms}	12.5 V	10.5 V		30 ns	90 ns	14 ns @ 25°C	13.5 A_{peak}	-14 A_{peak}	20.10.20, Rev. 2.0
TI	UCC5320SC	UL 1577 and VDE 0884-11	V_{ISO} = 3000 V_{rms}	12 V	11 V	33 V	n/a	60 ns	+ 12 ns (on) + 15 ns (off)	4.3 A_{peak}	-4.4 A_{peak}	SLLSER8F – JUNE 2017– REVISED JANUARY 2019
	UCC5350SB		V_{IOTM} = 4242 V_{peak}	8.7 V	8.0 V			65 ns	+ 35 ns (on/off)	8.5 A_{peak}	-10 A_{peak}	
	UCC5390SC			12 V	11 V					17 A_{peak}	-17 A_{peak}	
ON Semiconductor	NCD57080C	n.a.	3750 Vrms	12.9 V	12 V	32 V	40 ns	60 ns	+/- 15 ns	8 A_{peak}	-8 A_{peak}	Mar.-20, Rev. 0
ST	STGAP2HSMTR	n.a.	V_{IOTM} = 6000 V_{peak}	9.1 V	8.4 V	26 V	20 ns	75 ns	+/- 20 ns	4 A_{peak}	-4 A_{peak}	DS13393 Rev 2

Example: 600 W quarter-brick 48 V to 12 V full-bridge

See Application note:EiceDRIVER™ 2EDF7275K in telecom bricks

Table 3 Dead-time configuration settings for the efficiency measurements

Configuration	DT1	DT2	Difference to Config_A
Config_A	70 ns	40 ns	-
Config_B	75 ns	45 ns	+ 5 ns
Config_C	79 ns	49 ns	+ 9 ns
Config_D	101 ns	71 ns	+ 31 ns
Config_E	108 ns	78 ns	+ 38 ns



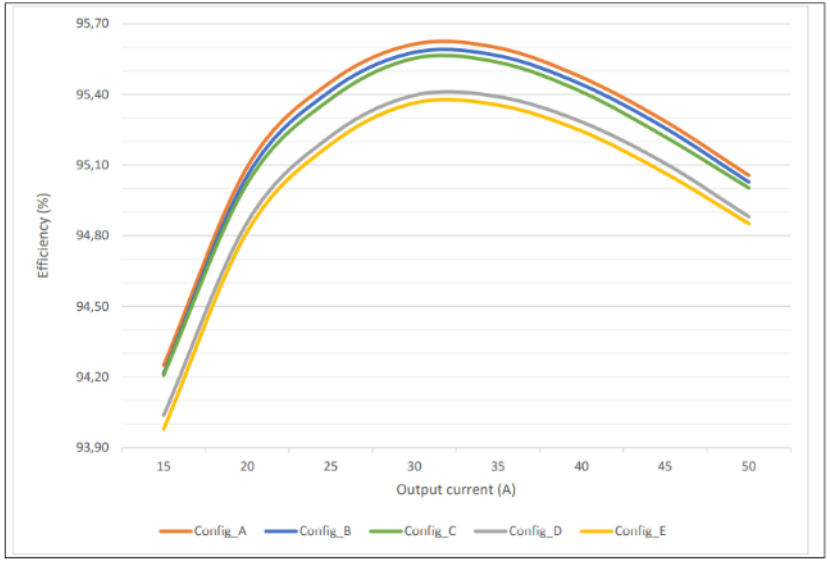


Figure 15 Efficiency measurement of the 600 W QB 48 V to 12 V FB-FB evaluation board at 48 V DC input voltage for the different dead-time configuration settings

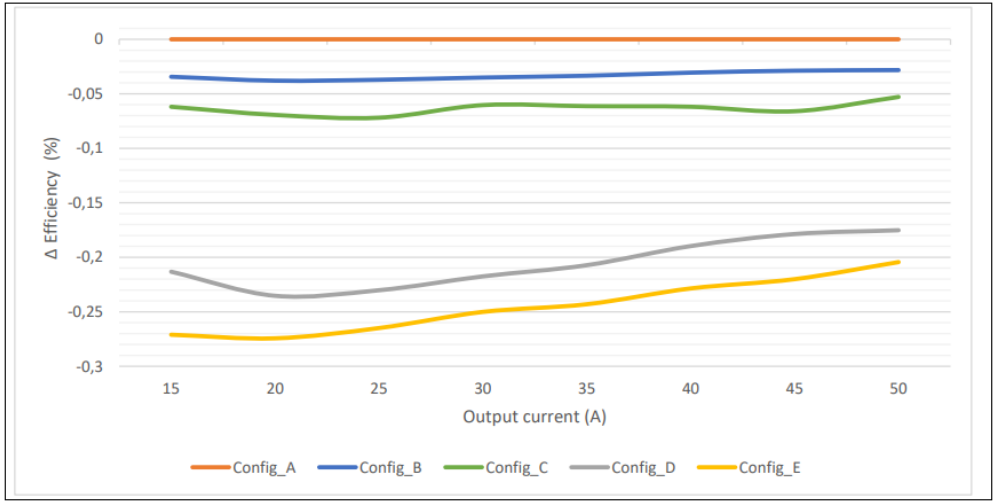
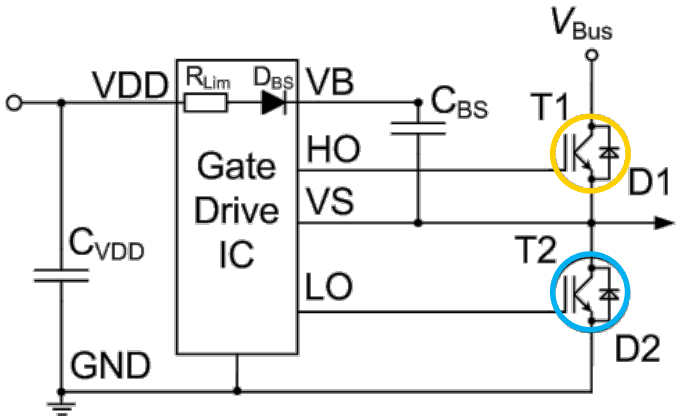


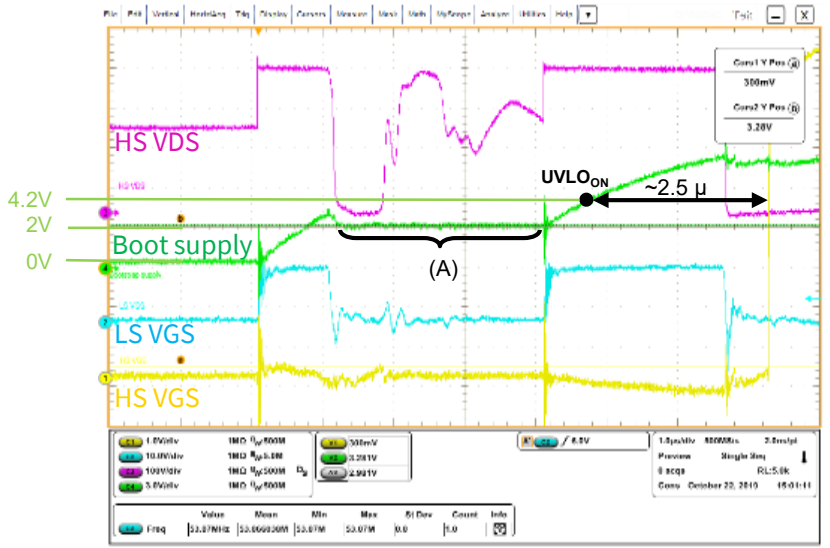
Figure 16 Differential efficiency measurement of the 600 W QB 48 V to 12 V FB-FB evaluation board at 48 V DC input voltage for the different dead-time configuration settings

UVLO (undervoltage lockout)

1EDB fast reaction time to UVLO events
Relevance in the end application – Bootstrap systems

- UVLO protects the FET from linear mode, so its level need to meet Vth
- Bootstrap issues during Startup, or burst-mode, while...
  - LS FET is switching
  - HS FET isn‘t switching, still in UVLO





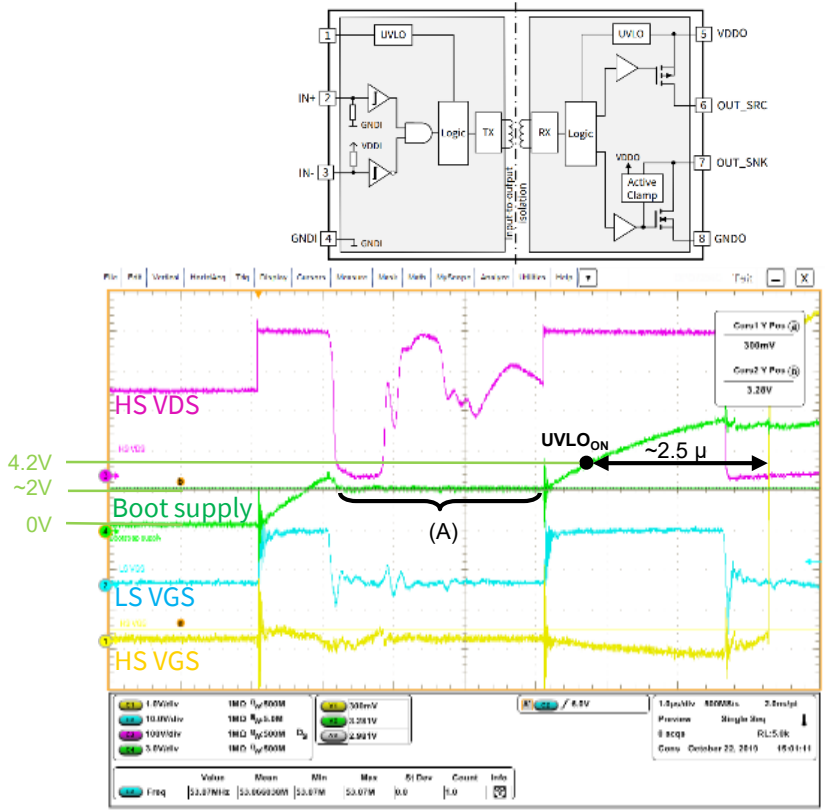
Example: burst-mode in 600W LLC eval board tested with 1EDB7275F

1EDB fast reaction time to UVLO events
Relevance in the end application – Bootstrap systems

- The start-up time in the datasheet depends on
  - the UVLO block activation time
  - the internal logic start-up time

- Here, the UVLO start-up time
  - measured ~2.5µs
    is lower than
  - datasheet specification 5µs

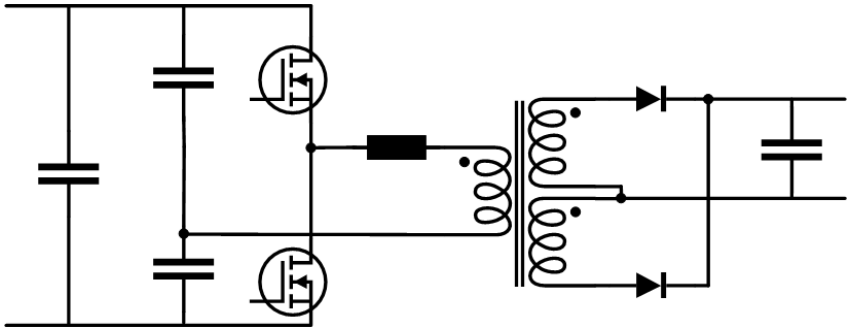
  since the internal logic has already started during the flat curve (A) and is ready to switch once the supply hits $UVLO_{ON}$

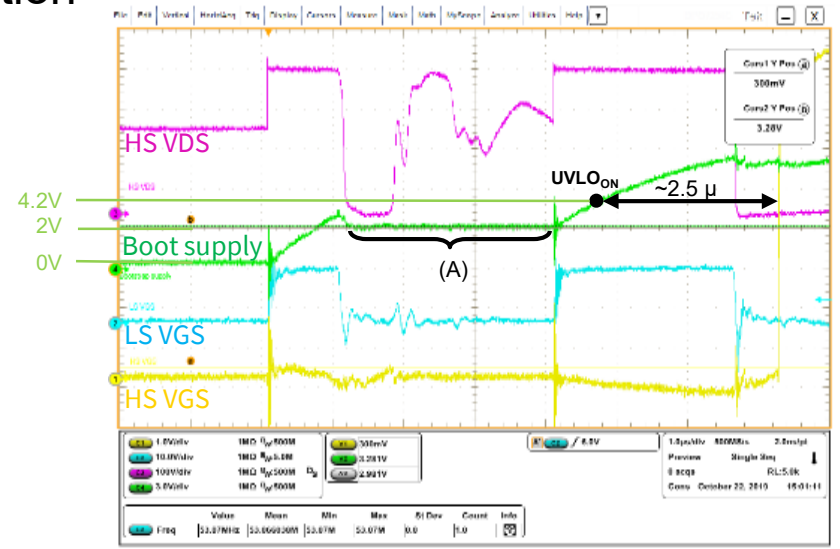


Example: burst-mode in 600W LLC eval board tested with 1EDB7275F

1EDB fast reaction time to UVLO events
Relevance in the end application – Bootstrap systems

- Quick UVLO system helps e.g. in LLC with split resonant cap
  - keeps cap voltages balanced, thus
  - helps preventing severe hard commutation





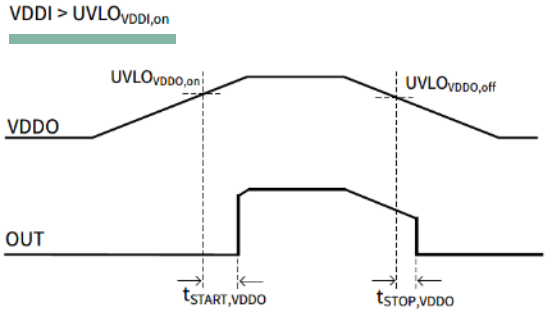
Example: burst-mode in 600W LLC eval board tested with 1EDB7275F

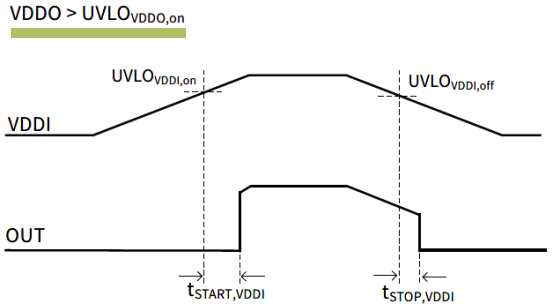
1EDB fast reaction time to UVLO events
Start-up and deactivation times

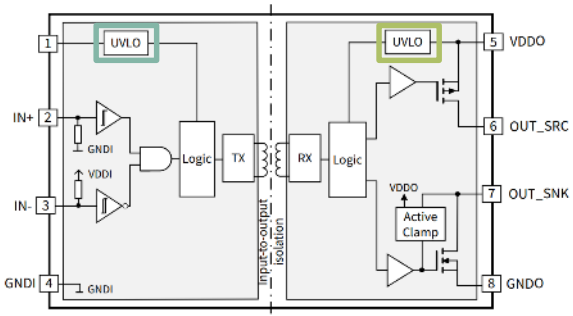
› Datasheet values:

Input-side start-up time	$t_{START,VDDI}$	–	3	–	µs	see **Figure 8**
Input-side deactivation time	$t_{STOP,VDDI}$	–	300	–	ns	see **Figure 8**
Output-side start-up time	$t_{START,VDDO}$	–	5	–	µs	see **Figure 9**
Output-side deactivation time	$t_{STOP,VDDO}$	–	125	–	ns	see **Figure 9**

New







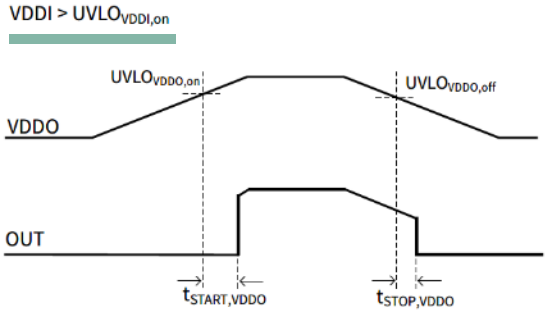
1EDB fast reaction time to UVLO events
Start-up and deactivation times

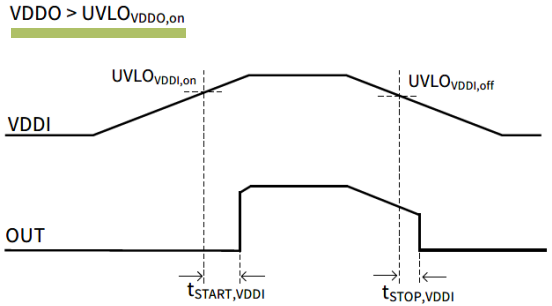
› Datasheet values:

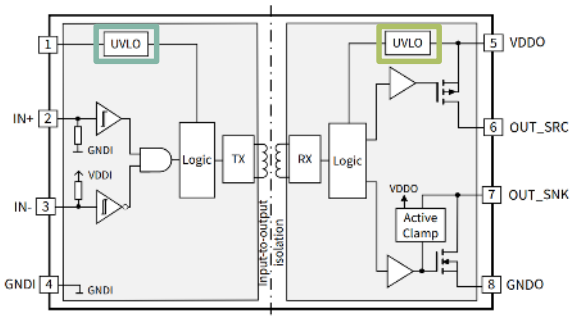
Input-side start-up time	$t_{START,VDDI}$	–	3	–	µs	
Input-side deactivation time	$t_{STOP,VDDI}$	–	300	–	ns	
Output-side start-up time	$t_{START,VDDO}$	–	5	–	µs	
Output-side deactivation time	$t_{STOP,VDDO}$	–	125	–	ns	

The input timing differs between the chips, but
The output timing of all EiceDRIVER™ 2EDi is the same

If the input pulse is sent after 5µs, the driver will react immediately since it is ready. If the pulse is not synchronized and has been set high before, a random 1.6 µs inaccuracy has to be considered on top due to the repetition scheme

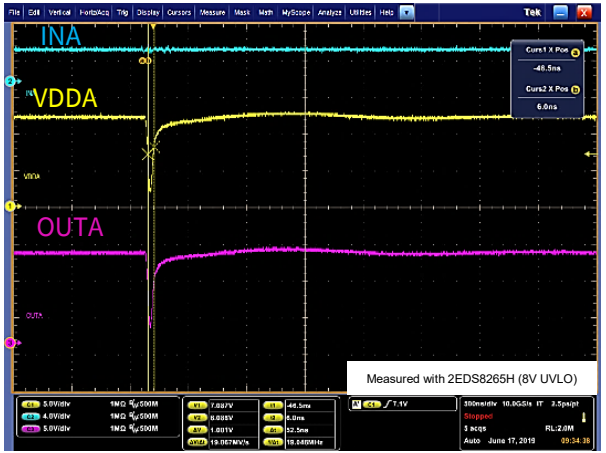




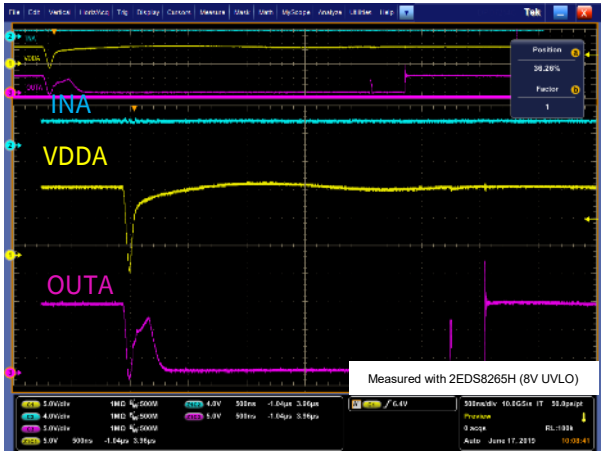


1EDB fast reaction time to UVLO events
Relevance in the end application – Reaction to glitches (1/2)

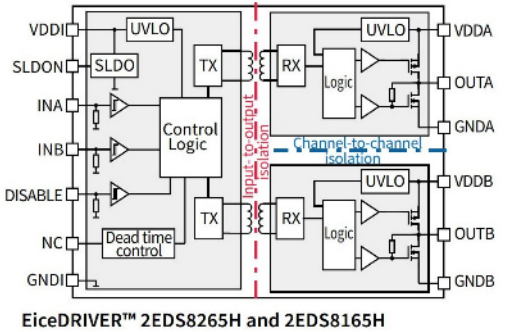
Output-side deactivation time	$t_{STOP,VDDO}$	–	125	–	ns	see **Figure 9**



Glitches of few of ns (switching noise)
filtered out



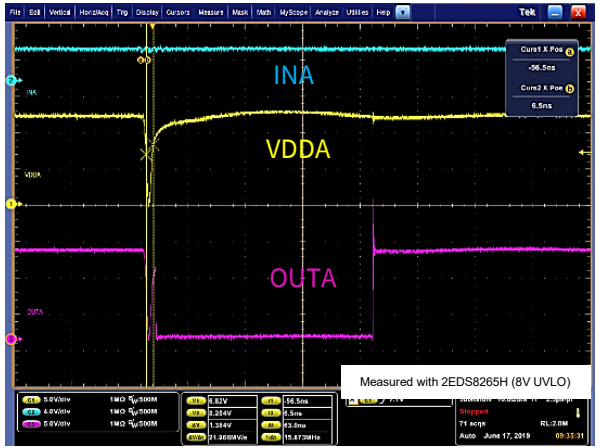
Glitches longer than hundreds of ns
pass through

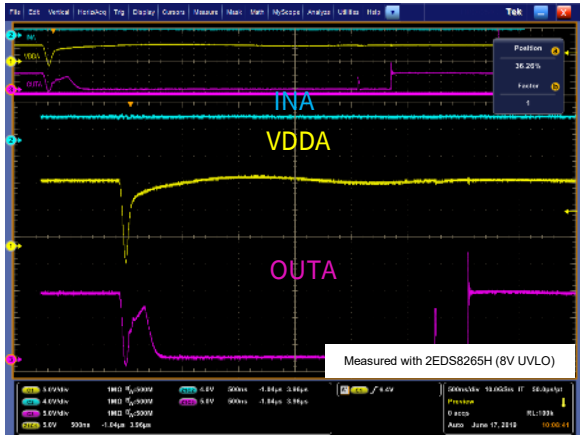


EiceDRIVER™ 2EDS8265H and 2EDS8165H

1EDB fast reaction time to UVLO events
Relevance in the end application – Reaction to glitches (2/2)

- For glitches being able to deactivate the UVLO-block, the reaction time of the drivers depends on how fast, how deep and how long the glitch is.
  - The minimum reaction time of the driver is given by the UVLO block activation (~2.5µs)
  - The maximum reaction time of the driver is given by the maximum start-up time (~5µs) (UVLO+LogicBlock).





- 1EDBx275F and 2EDi are able to react within one pulse of 5µs or less to supply drop, e.g. due to noise, enabling fast recovery of normal system operation

- Fast UVLO reaction times…
  - enable fast recovery of normal system operation
  - helps ensuring stable system operation
  - especially important, e.g., in high-density brick applications to keep the output regulation.

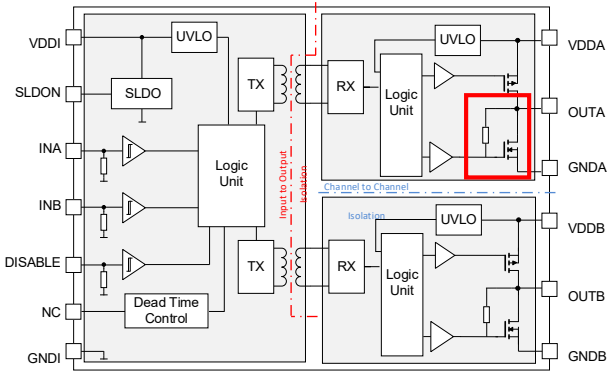
Fast active output clamping

New Active Output Clamping (for VDDO < UVLO)

- Motivation:
  - During startup, while $V_{dd\_highside}$<UVLO, high dV_{DS}/dt can cause V_G to be lifted above V_{th}
  - This can cause erratic turn on, thus shoot-through
- Wanted:
  - Fast clamping of the output
  - Active already at lowest possible driver-supply voltage V_{DDA} resp. V_{DDB}

Slow RC output clamping

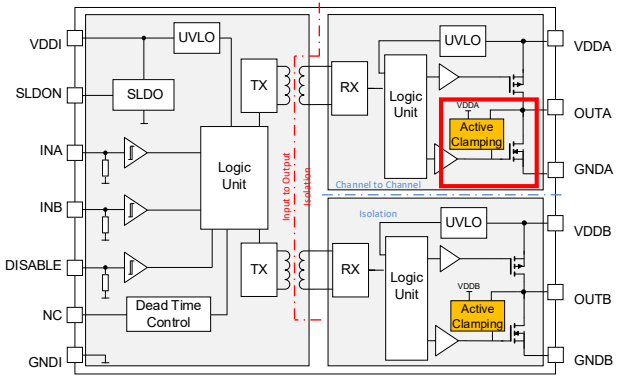
(old 2EDi marking A, some competitors products)



~ **µs** time constant to activate clamping

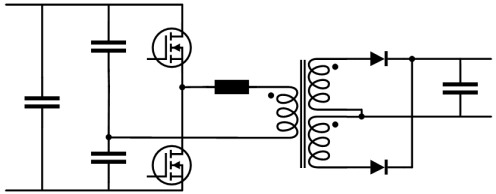
Fast active output clamping

(EiceDRIVER™ 1EDB, new 2EDi marking B)



~ **ns** time constant to activate clamping

New Active Output Clamping (for VDDO < UVLO)
Benefit in the end-application



Critical topology/condition

- LLC with split resonant cap
- Bootstrap circuit used
- Any condition when bootstrap supply is below UVLO (start-up, burst mode)

Slow RC output clamping

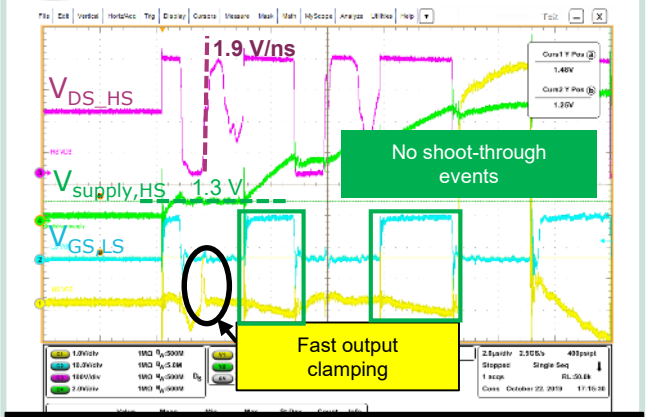
(old 2EDi marking A, some competitors products)

Test-board: Customer LLC board, start-up

Shoot-through due to driver slow output clamping for boot supply below UVLO

Fast active output clamping

(EiceDRIVER™ 1EDB, new 2EDi marking B)



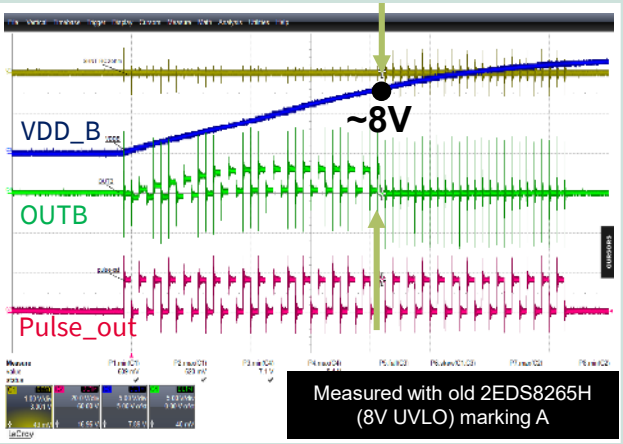
Test-board: Infineon 600W LLC board readapted with 1EDB8275F, burst-event

No shoot-through thanks to driver fast output clamping for boot supply below UVLO

New Active Output Clamping (for VDDO < UVLO) In action…

Slow RC output clamping

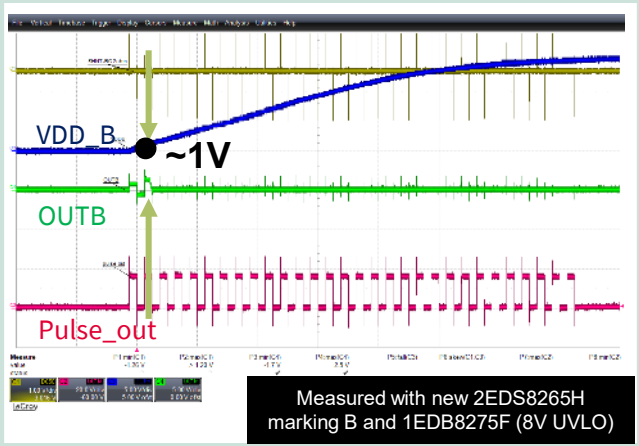
(old 2EDi marking A, some competitors products)



Late clamping activation: Output clamping activates when the supply approaches the UVLO level (e.g. **8V**)

Fast active output clamping

(EiceDRIVER™ 1EDB, new 2EDi marking B)



Early clamping activation: Output clamping activates when the supply approaches **1V**

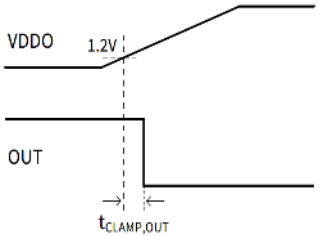
› Results from component verification measurements; pulse (Pulse_out) forced on the Gate Driver output (OUT) and supply (VDD_B) raised with controlled ramp; due to selected switching frequency, slow clamping mechanisms are not visible

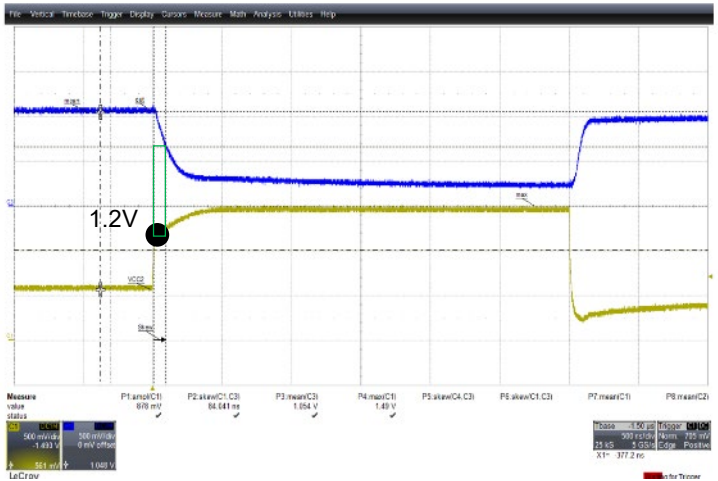
New Active Output Clamping (for VDDO < UVLO)
1EDB clamping activation time

Activation time of output clamping in UVLO condition [3]	$t_{CLAMP,OUT}$	–	20	–	ns	see **Figure 10**

3) parameter not subject to production test - verified by design / characterization

New





- Parameter measured raising the 1EDB output supply (fast ramp) and forcing 1V on the output.
- The activation time is the time needed from the driver to start clampimg the output after the supply has reached the trigger value (~1V)

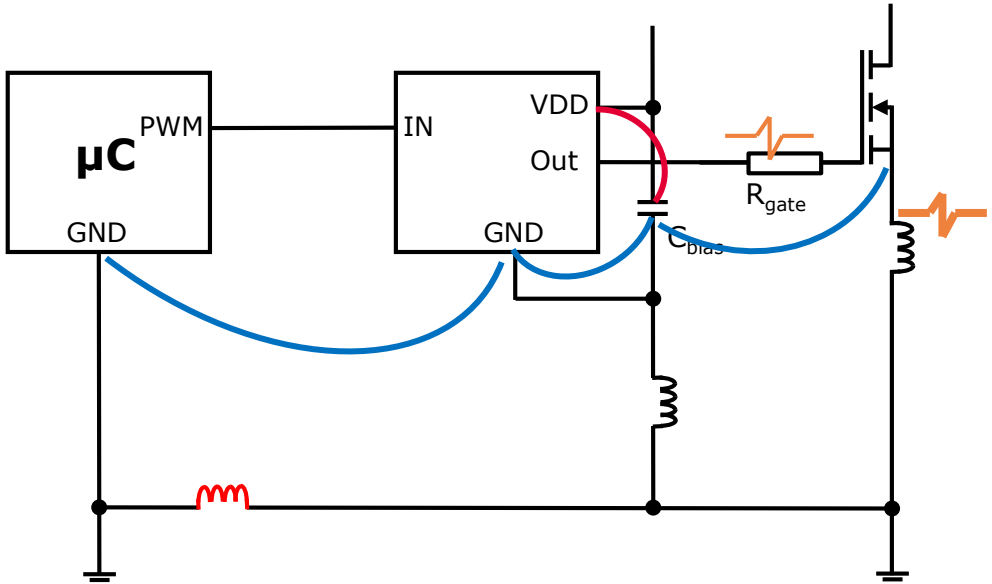
Key take-aways

- If you compare datasheets or look for a suitable driver:
  - Don‘t be fooled by the cover-page parameters
  - Compare currents wrt. to their load type and voltage spec.
  - Compare timings wrt. their spec-conditions
  - Focus on special application requirements like
    - UVLO level, precision, timing, speed for ON and OFF
    - Timing precision of the driver

Layout considerations

Layout considerations

- Keep Signal-GND away from Power-GND
- Use short, thick traces
- Use local, 5x wider traces underneath the signal as return
- Do not span areas, they‘re nice antennas



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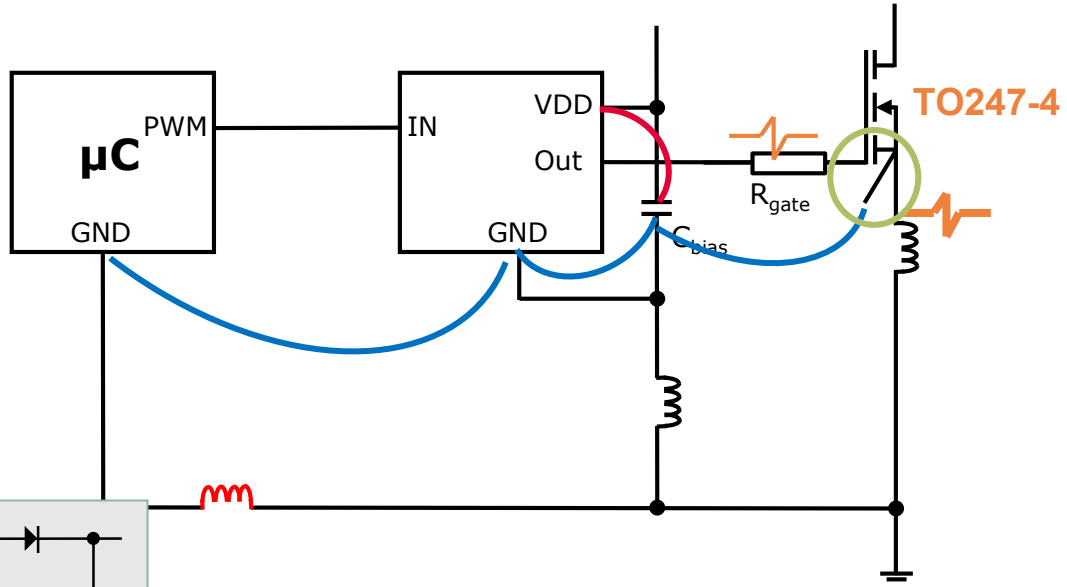
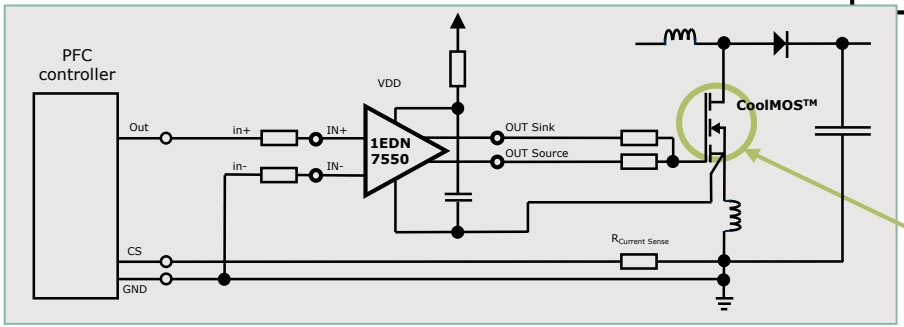
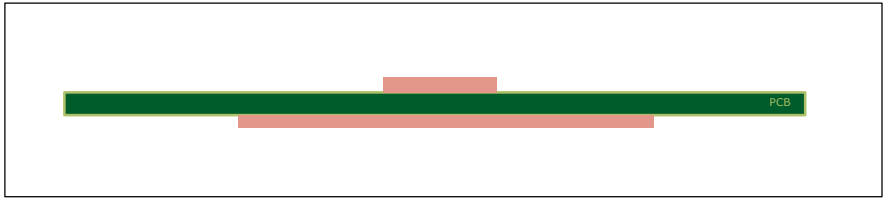


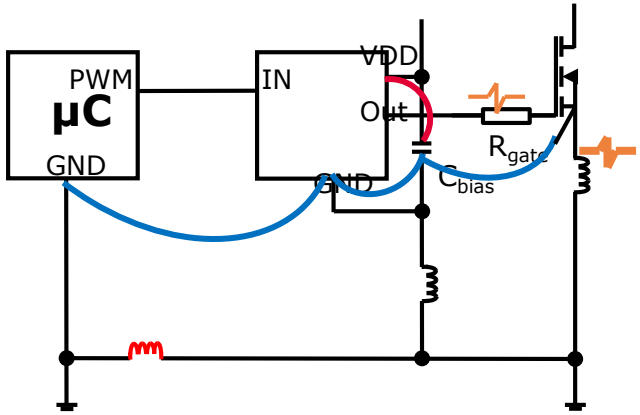


- GND connection on 4pin device

Layout considerations

- Keep Signal-GND away from Power-GND
- Use short, thick traces with low impedance return
- Use local, 5x wider traces underneath the signal as return.



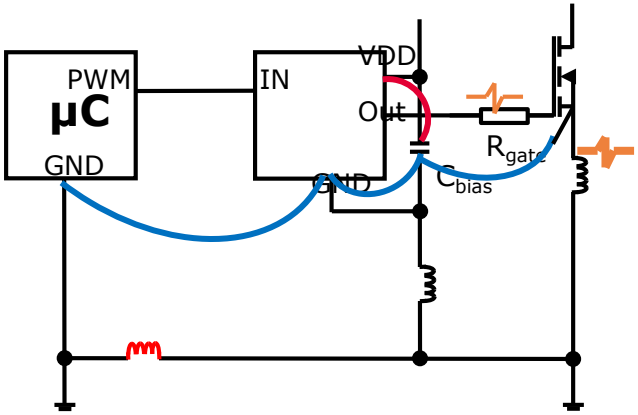


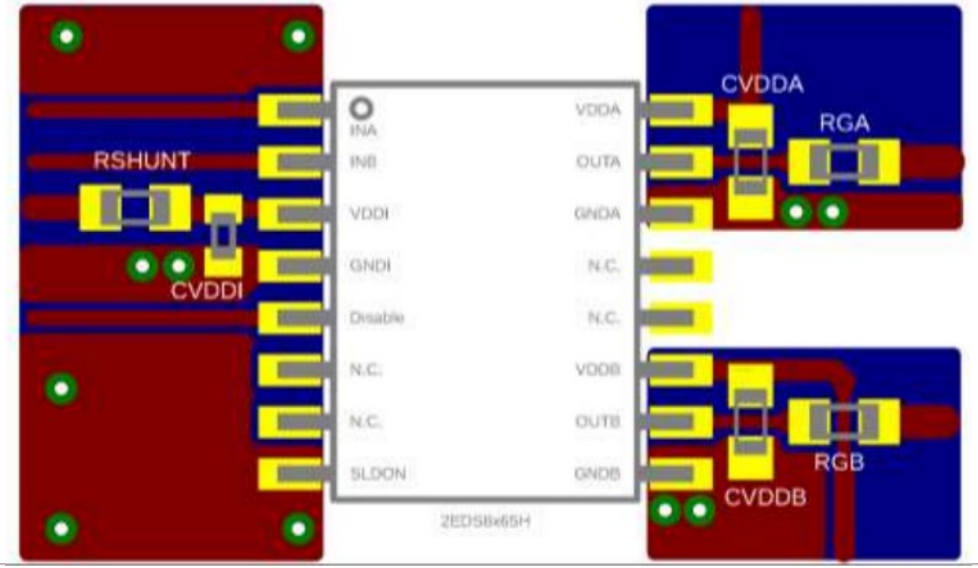
- With the signal on TOP and a wide return on BOTTOM side, a very low impedance path (not only low ohmic) is defined, including a catch for E-fields.

- Do not, ***never***, use complete GND-Plane for power-returns as it injects noise to everything.

Layout considerations

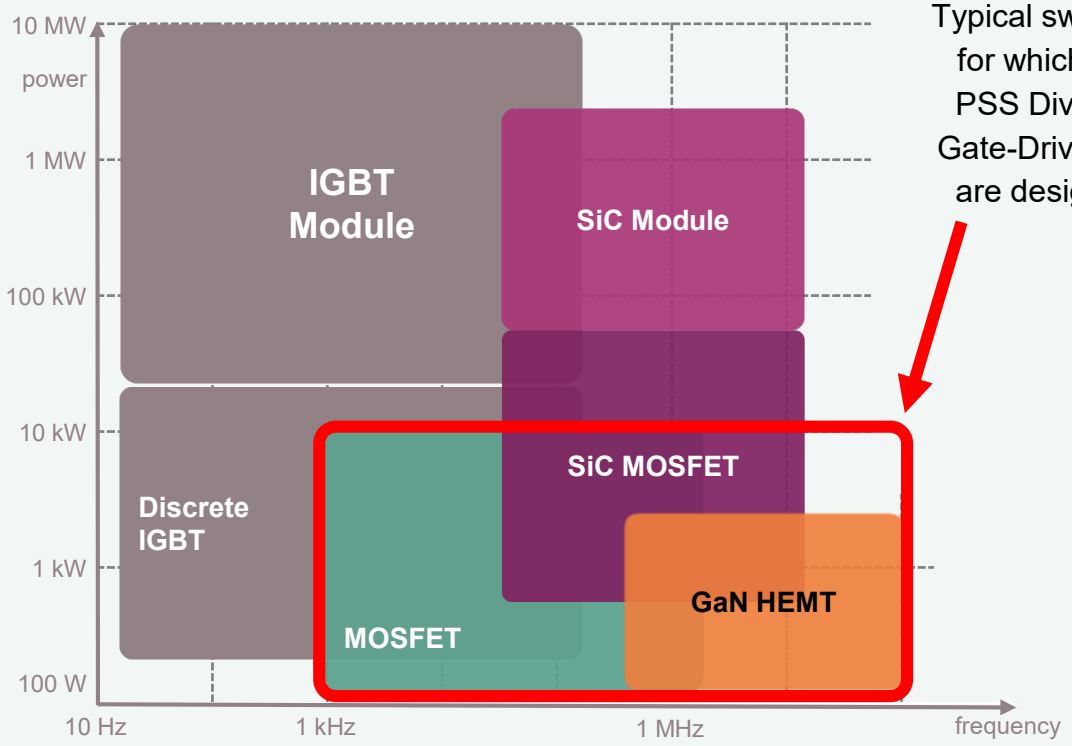
- Keep Signal-GND away from Power-GND
- Use short, thick traces with low impedance return
- Use local, 5x wider traces underneath the signal as return





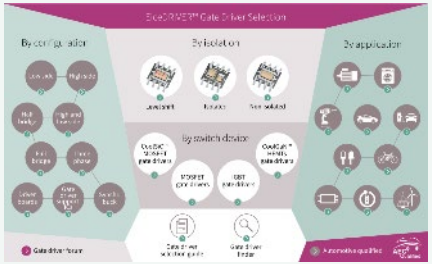
Portfolio – Overview

- prelude -



Typical switches for which the PSS Division Gate-Driver ICs are designed

Please visit
www.infineon.com/gatedriver
for entire gate-driver IC portfolio



Legend

- in production
- in development
- in concept stage

▼ ES ▼ MP

Gate Driver IC Nomenclature of PSS Division
- Guideline -

Number of channels
e.g., 1, 2, 6

ED **= EiceDRIVER™**

Isolation class*
N = Non-isolated, e.g. low-side or True Differential Inputs
L = Level-shift junction isolation
F = Functional isolation
B = Basic isolation VDE certified or single protection (UL1577)
S = Reinforced isolation certified VDE 0884-10 (exp.) & EN 62368-1
R = Reinforced isolation certified VDE 0884-11 & EN 62368-1
(and in future IEC 60747-17)

UVLO**
6 = 12.2 V
7 = 4.2 V
8 = 8.0 V
9 = 14.9 V

Output current***
1 = 1A/2A
2 = 4A/8A

Family ID
e.g.
2 = 2EDN
5 = 2EDR, 2EDB
6 = 2EDS
7 = 2EDF

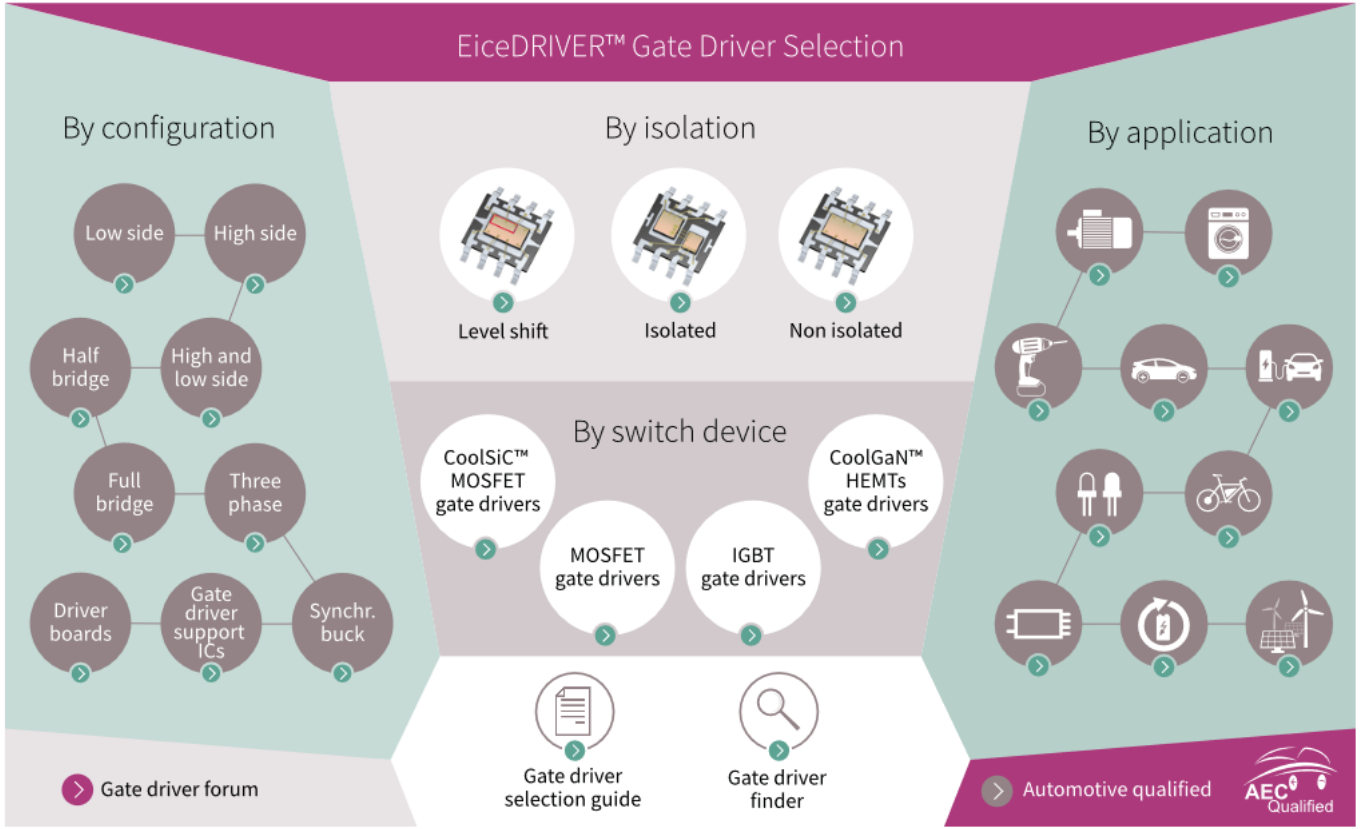
Control inputs
Non-isolated drivers:
1EDN: 1 = single, 2 = spit output
2EDN: 3 = inverted, 4 = direct input

Galvanically isolated drivers******:
3 = PWM input w. DTC or TNEG
5 = INA, INB w/o STP/DTC + DIS
6 = INA, INB with STP + EN
7 = INA, INB with STP + DIS
8 = INA, INB with STP/DTC option + EN
9 = INA, INB with STP/DTC option + DIS

Package type
A = LGA 4x4 mm
B = SOT-23
F = DSO 150mil, 8-/16-pin
G = SON
H = DSO 300mil, 16-pin
K = LGA 5x5 mm
R = TSSOP (“mini DSO-8”)
U= TSNP
X = DSO 300mil, 14-pin
Y = DSO 150mil, 14-pin

* please refer to data-sheet for actual cerification status
** typ. on-threshold
*** @ Vdd = 12V, Vout = 5V
**** DIS is the default, repective number is used even if a dedicated pin is not avail.

Navigating the Infineon Gate-Driver IC world
Visit www.infineon.com/gatedriver



Every Switch needs a Driver

eicedriver@infineon.com

"Common DNA" through-out the portfolio for High System Efficieny and Robust & Save Operation

		Low-side		Non-isolated	Isolated			
		1-channel	2-channel	1-channel	1-channel	2-channel		
Product examples		1EDN7511B	2EDN7524R	1EDN7550B	1EDB7275F	2EDF7275F		
Low resistance rail-to-rail output stages	source	0.85 Ω / 4 A	0.7 Ω / 4 A	0.85 Ω / 4A	0.95 Ω / 4 A	0.85 Ω / 4 A	**Minimizes MOSFET switching losses**	**High System Efficiency**
	sink	0.35 Ω / 8 A	0.55 Ω / 4 A	0.35 Ω / 8 A	0.48 Ω / 8 A	0.35 Ω / 8 A		
Input-to-output propagation delay accuracy	on	+ 6 ns	+ 4 ns	+ 10 ns	+ 4 ns	+ 7 ns	**Minimizes dead-time losses**	
	off	- 4 ns	- 4 ns	- 7 ns	- 4 ns	- 6 ns		
Input robustness	abs. max.	- 10V	- 10V	+/- 150V (TDI)	- 5V	- 5V	**Noise margin**	**Robust and Save System Operation**
Fast output clamping			20 ns	20 ns	20 ns	20 ns	**Avoids half-bridge shoot-through during boot-strapped start-up**	
UVLO options	typ. off threshold	3.9 V 7.0 V	3.9 V 7.0 V	3.9 V 7.0 V 14.4 V	3.9 V 7.0 V 11.5 V, 14.4 V	3.9 V 7.0 V 12.9 V, 14.4 V	**Reduces risk of thermal overstress of power switch, if auxiliary supply drops**	
Reverse current robustness	abs max.	5 A_{peak}	5 A_{peak}	5 A_{peak}	5 A_{peak}	5 A_{peak}	**No need for Schottky diodes to protect gate-driver output**	
Galvanic isolation		n.a.			UL 1577, VDE 0884		**Rugged ground-loop separation**	
CMR / CMTI				Truly Differential Inputs	> 300 V/ns	> 150 V/ns	**Immune against switching noise**	

Low-Side Gate-Driver ICs
Portfolio and Roadmap

(Q2CY21; PL21B)

1-ch

1EDN Family

4 A / 8 A
SOT23-5
SOT23-6
WSON-6

1EDN7512B
1EDN7511B
1EDN8511B
1EDN7512G

1EDN Exp_1

New: 12 A_{src} / 25 A_{sink} (VDD up to 12 V)

WSON-6

TSNP-6

Source-down OptiMOS in IBC & HSC with switched capacitor topologies

Center-tapped SR in Telco DCDC-Bricks & High-power SMPS

2-ch

2EDN Family

4 A / 4 A or 5 A / 5 A
DSO-8
TSSOP-8
WSON-8

2EDN752xF
2EDN852xF
2EDN752xR
2EDN852xR
2EDN752xG
2EDN7424x

2EDN Expansion1

New: 20 ns fast output clamp
New: 2 µs UVLO start-up time
New: SOT23-6
New: TSNP-6

now* May-21*

*DSO, TSSOP, SOT

In Production **2021** **2022**

Truly Differential Input Gate-Driver ICs
Portfolio and Roadmap

(Q2CY21; PL21B & PL88I)

1-ch

1EDN-TDI Family

Truly Differential Inputs

4 A / 8 A

SOT23-6

TSNP-6

1EDN7550B

1EDN8550B

1EDN7550U

In Production

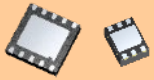
1EDN71x6 Family for 100 V GaN

TDI for 150 V CMR

DT selectable

Negative charge pump option

3x3 mm SON-10, 1.8x1.8 mm TSNP-7



Feb-21 Apr-21

2021

1EDN-TDI Exp_1

New: Eliminates external R_{CM}

SOT23-6: up to +/-150 V

TSNP-6: +/- 120 V

FB-SR in Telco DCDC Bricks

IBC & HSC in switched capacitor topologies

Boost-PFC w. KelvinSource MOSFET

Totem-pole PFC

FB-Sync Rec

HB in Battery powered motor drives

PV optimizer

2022

Junction Isolated Gate-Driver ICs
Portfolio and Roadmap

(Q2CY21; PL88I)

2-ch

2EDL8x2x Family
120 V int. boot-strap diode
2 A to 4 A
TDI option
SON-8 4x4

2EDL802xG
2EDL812xG
2EDL8012G
2EDL8112G

Wireless Charging Driver
60 V int. boot-strap diode
2 A
SON-10 4x4

WDCSC0006

2EDL8x2x Exp1
NEW: SON-10 3x3 (telco DCDC)
May-21 Nov-21

HB 120 V GaN driver
120 V int. boot-strap diode
Active Miller Clamp
TSNP-12 2x2
Aug-21 Q2-22

HB 120 V telco DCDC Driver
120 V internal boot-strap diode
SON-8 4x4
SON-10 3x3
DSO-8 (solar and SR)
Jan-22 Oct-22

6-ch

6EDL7141
70 V 3-phase Smart **Motor Driver**
VQFN-48 7x7
Oct-20 May-21

In Production **2021** **2022**

Galvanically Isolated Gate-Driver ICs
Portfolio and Roadmap

(Q2CY21; PL21B & PL88I)

1-ch

1EDi-GaN

DSO-16 300mil
DSO-16 150mil
LGA-13 5x5

1EDS5663H
1EDF5673F
1EDF5673K

1EDB-Family

+5.6 A source / -10.2 A sink
20 ns fast output clamp
5 µs UVLO start-up time
4 V to 15 V UVLO options
300 V/ns CMTI
V_{ISO} = 3 kV_{rms} (UL1577)
150 mil DSO-8

1EDB6275F
1EDB7275F
1EDB8275F
1EDB9275F

2-ch

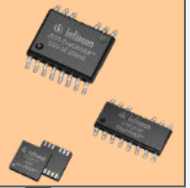
2EDi Family

1 A / 2 A, 4 A / 8 A
DSO-16 300mil
DSO-16 150mil
LGA-13 5x5

2EDS9265H
2EDS8265H
2EDS8165H
2EDF9275F
2EDF7275F
2EDF7175F
2EDF7275K
2EDF7235K

2EDi Expansion1

New: STP, DTC (option)
New: 20 ns fast output clamp
New: 2 µs UVLO start-up time
New: 300 V/ns CMTI
New: VDE 0884-11
New: DSO-14 300mil
New: DSO-14 150mil
New: LGA-13 4x4



May-21 Oct.-21

In Production **2021** **2022**

2-channel isolated gate-driver IC Portfolio and Roadmap in detail

Product	Package		Isolation Certification	Outputs stage		Controls		
	Type	Pins		source/sink	UVLO	inputs	STP/DTC option	DIS/EN
2EDS8165H	300mil DSO	16 pin	V_{IOTM} = 8kV$_{pk}$ VDE-10	1A / 2A	8V	INA, INB	no	DIS
2EDS8265H	300mil DSO	16 pin	V_{IOTM} = 8kV$_{pk}$ VDE-10	4A / 8A	8V	INA, INB	no	DIS
2EDS9265H	300mil DSO	16 pin	V_{IOTM} = 8kV$_{pk}$ VDE-10	4A / 8A	13V	INA, INB	no	DIS
2EDR8259H	300mil DSO	16 pin	V_{IOTM} = 8kV$_{pk}$ **VDE-11**	4A / 8A	8V	INA, INB	**yes**	DIS
2EDR7259X	300mil DSO	**14 pin**	V_{IOTM} = 8kV$_{pk}$ **VDE-11**	4A / 8A	4V	INA, INB	**yes**	DIS
2EDR8259X	300mil DSO	**14 pin**	V_{IOTM} = 8kV$_{pk}$ **VDE-11**	4A / 8A	8V	INA, INB	**yes**	DIS
2EDR9259X	300mil DSO	**14 pin**	V_{IOTM} = 8kV$_{pk}$ **VDE-11**	4A / 8A	**15V**	INA, INB	**yes**	DIS
2EDF6258X	300mil DSO	**14 pin**	**functional**	4A / 8A	**12V**	INA, INB	**yes**	**EN**
2EDF7175F	150mil DSO	16 pin	1.5kV$_{DC}$ functional	1A / 2A	4V	INA, INB	no	DIS
2EDF7275F	150mil DSO	16 pin	1.5kV$_{DC}$ functional	4A / 8A	4V	INA, INB	no	DIS
2EDF9275F	150mil DSO	16 pin	1.5kV$_{DC}$ functional	4A / 8A	13V	INA, INB	no	DIS
2EDB8259F	150mil DSO	16 pin	**V_{ISO} = 3kV$_{rms}$ UL1577**	4A / 8A	8V	INA, INB	**yes**	DIS
2EDB7259Y	150mil DSO	**14 pin**	**V_{ISO} = 3kV$_{rms}$ UL1577**	4A / 8A	4V	INA, INB	**yes**	DIS
2EDB8259Y	150mil DSO	**14 pin**	**V_{ISO} = 3kV$_{rms}$ UL1577**	4A / 8A	**8V**	INA, INB	**yes**	DIS
2EDB9259Y	150mil DSO	**14 pin**	**V_{ISO} = 3kV$_{rms}$ UL1577**	4A / 8A	**15V**	INA, INB	**yes**	DIS
2EDF7275K	5x5 LGA	13-pin	1.5kV$_{DC}$ functional	4A / 8A	4V	INA, INB	no	DIS
2EDF7235K	5x5 LGA	13-pin	1.5kV$_{DC}$ functional	4A / 8A	4V	INA, INB	DTC	DIS
2EDB7259K	5x5 LGA	13-pin	**V_{ISO} = 2.5kV$_{rms}$ UL1577**	4A / 8A	4V	INA, INB	**yes**	DIS
2EDB8259K	5x5 LGA	13-pin	**V_{ISO} = 2.5kV$_{rms}$ UL1577**	4A / 8A	**8V**	INA, INB	**yes**	DIS
2EDB7259A	**4x4 LGA**	13-pin	**V_{ISO} = 2.25kV$_{rms}$ UL1577**	4A / 8A	4V	INA, INB	**yes**	DIS
2EDB8259A	**4x4 LGA**	13-pin	**V_{ISO} = 2.25kV$_{rms}$ UL1577**	4A / 8A	**8V**	INA, INB	**yes**	DIS

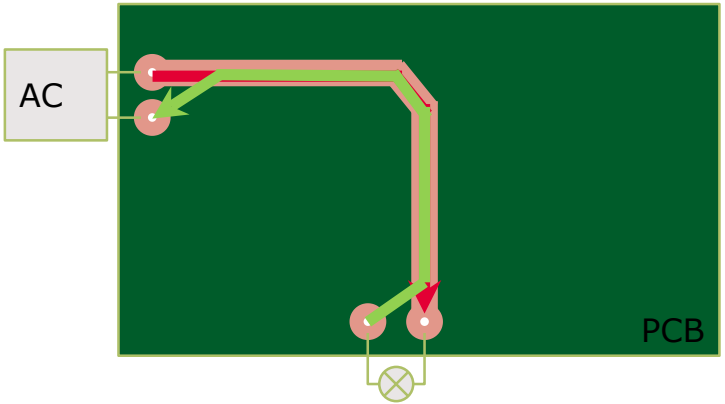
Note: VDE 0884-10 expired, but IEC 62368-1 survives

Part of your life. Part of tomorrow.

Addendum - layout

Exkurs – Layout – the way AC flows

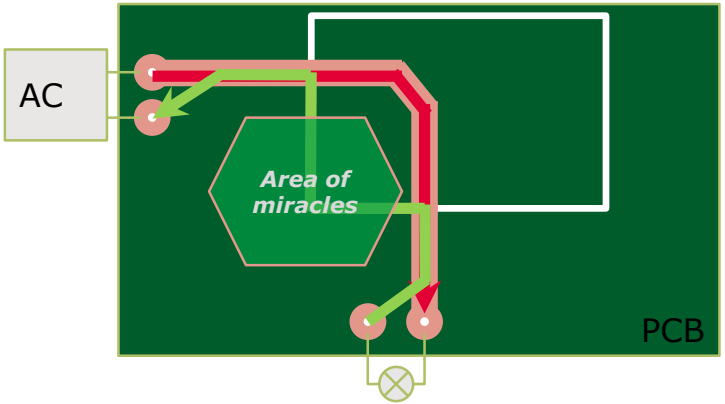
› Complete GND plane assumed



› AC return current
  – uses the low impedance trace
  – not the low ohmic trace

Layout – the way AC flows

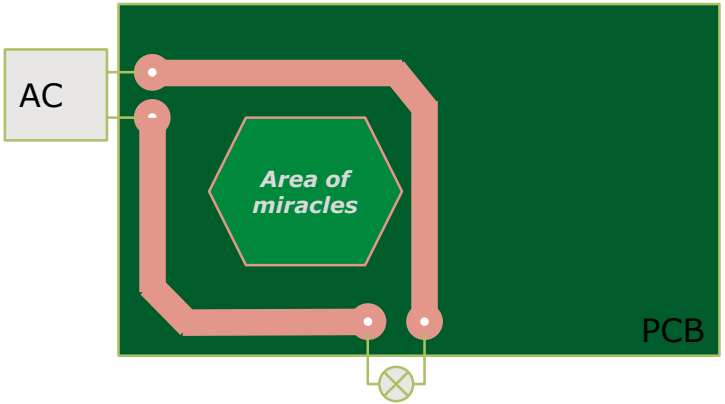
› Fractured GND plane assumed



› AC return current
  – uses an unknown way
  – induces *wonderful* signals into parts not intended to be meant

Layout – the way AC flows

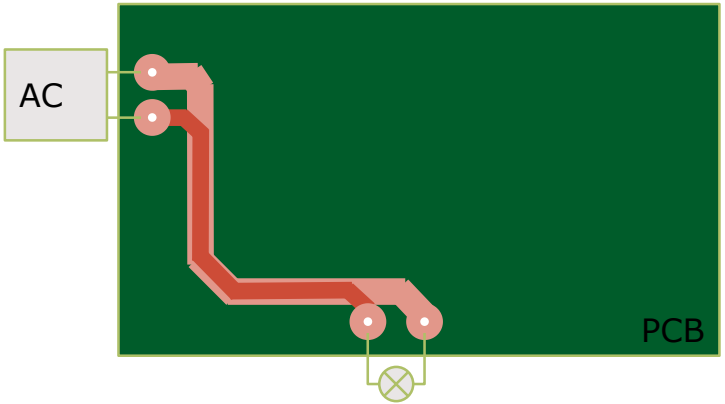
› Fractured or complete GND plane assumed



› AC return current
  – forced in a known path, but
  – spans a huge antenna area, generating radiated noise

Layout – the way AC flows

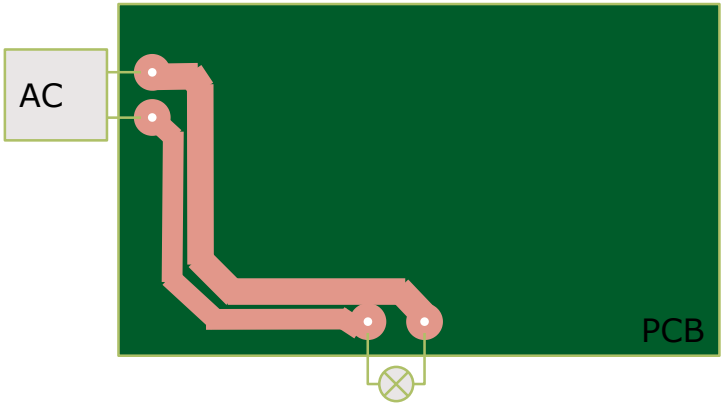
› Fractured or complete GND plane assumed



› AC return current
  – forced in a low impedance, non-disturbing path

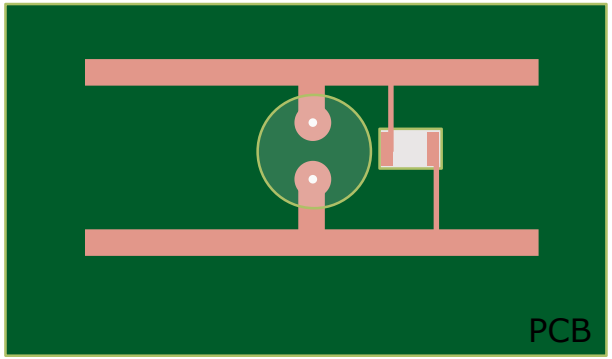
Layout – the way AC flows

› Fractured or complete GND plane assumed



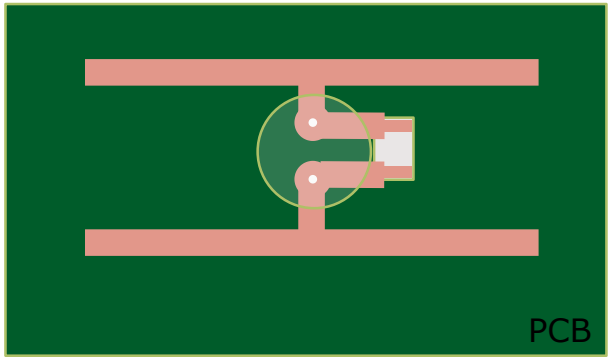
› AC return current – alternative on single side PCB
  – forced in a low impedance, non-disturbing path

Exkurs2 – Layout – blocking caps - Example



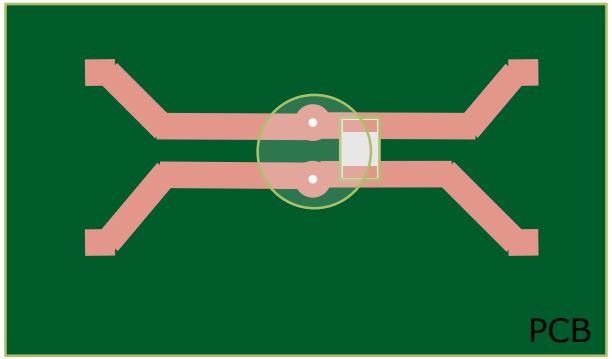
- Absolutely horrible …
  - C13 (100nF) is de-facto *not connected* due to trace impedance

Exkurs2 – Layout – blocking caps - Example



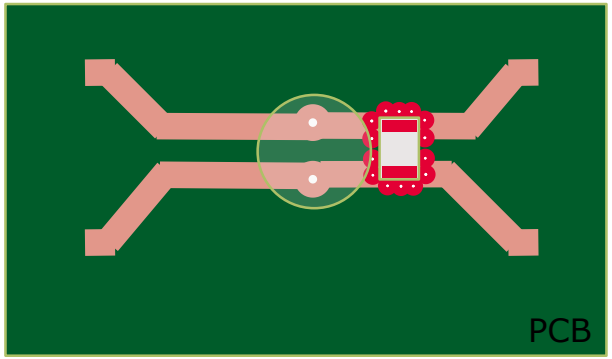
- Nearly absolutely horrible …
  - C13 (100nF) is de-facto *not connected* due to trace impedance

Exkurs2 – Layout – blocking caps - Example



- I‘d prefere this way!
  - Current forced to use both caps
  - Small spanned area
  - Low impedance traces

Exkurs2 – Layout – blocking caps - Example



- I'd prefer this way, if you really need the other pcb-side!
  - Please, place the cap onto the trace, avoid contacts
  - If you really need contacts, use lots of them