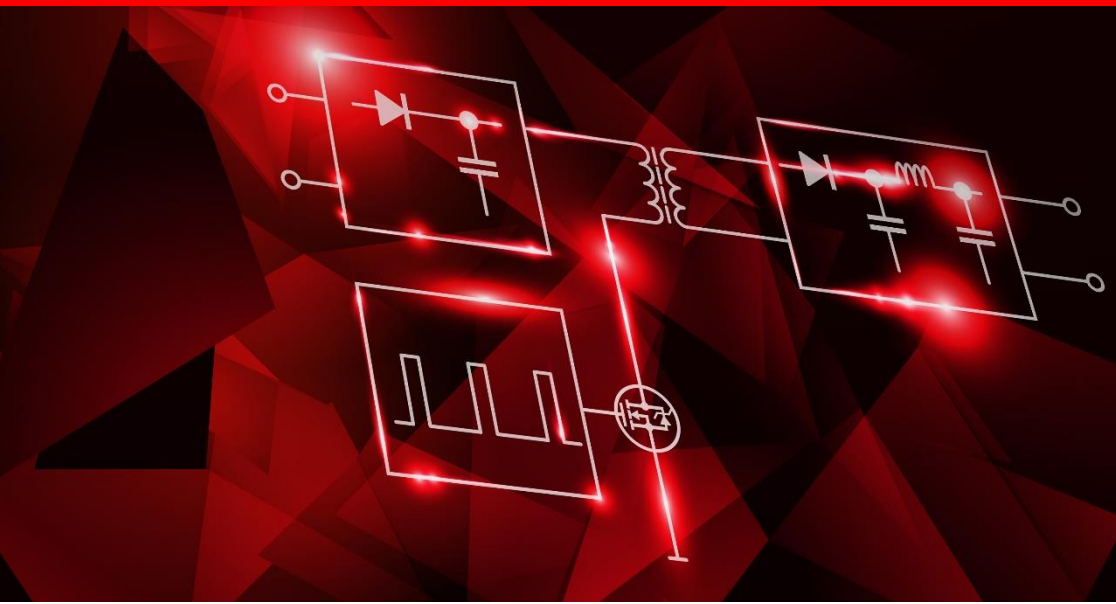
RUTRONIK POWER

RUTRONIK ELECTRONICS WORLDWIDE



RUTRONIK TechTalk meets Gate Driver

Where to start for a gate drive circuit design?

Dr. Wolfgang Frank | Lead Principal Gate Driver ICs

Infineon Technologies AG

Learning objectives

- Know how to calculate a reference gate resistance value for example a SiC MOSFET
- Identify suitable gate driving ICs based on peak current and power dissipation requirements
- Find out how to fine-tune the gate resistance value in laboratory environment

Your trainer today

Dr. Wolfgang Frank
Technical Marketing
Gate driver ICs

Agenda

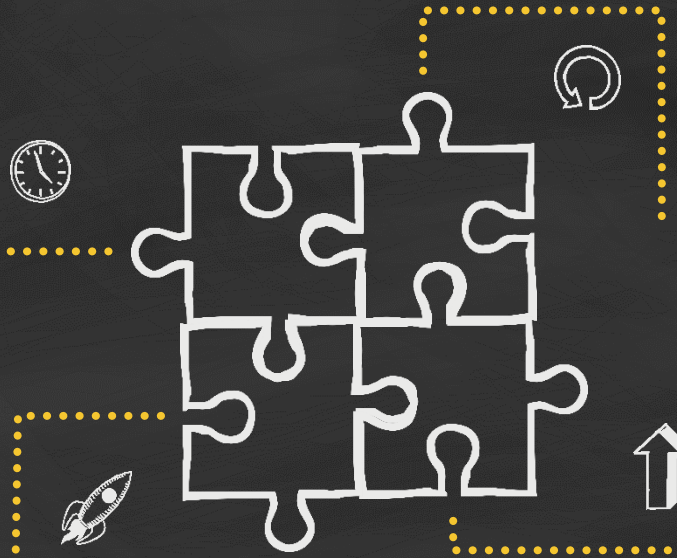
1. Power transistor’s characteristics
2. Gate driver design step-by-step and calculation flow

Agenda

1 Power transistor’s characteristics

2 Gate driver design step-by-step and calculation flow

Main characteristics of power transistors



Fast switching devices

Reach up to 50 V/ns (or more)

Properties of body diode

Freewheeling body diode:

› with little Q_R

› with high V_F

On-state performance

Short circuit performance sacrifice

Parasitic turn-on

May need negative gate voltage to stay in off-mode

Main characteristics of power transistors

Fast switching devices

Reach up to 50 V/ns (or more)

Properties of body diode

Freewheeling body diode:

› with little Q_R

› with high V_F

Gate driver circuits and ICs should support all these characteristics!

On-state performance

Short circuit performance sacrifice

Parasitic turn-on

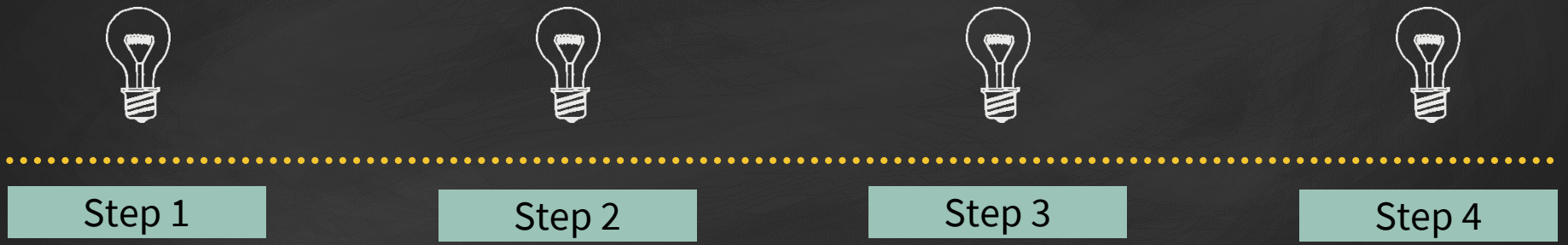
May need negative gate voltage to stay in off-mode

Agenda

1 SiC MOSFETs characteristics and Infineon gate driver IC offering

2 Gate driver design step-by-step and calculation flow

Design steps



Design steps

Calculate peak I_g based on the power transistor's datasheet
Select suitable gate driver based on peak current




Step 1

Peak current and gate driver IC selection

Step 2

Step 3

Step 4

Design steps

Calculate gate resistor based on your application's gate voltage swing
Target: get the same switching performance as in datasheet




Step 1	Step 2	Step 3	Step 4
Peak current and gate driver IC selection	Adaptation of gate resistor value to the application conditions		

Design steps

Calculate internal power dissipation of the IC
Calculate the gate resistor's power dissipation
Verify both power dissipations with datasheet values




Step 1

Peak current and gate driver IC selection

Step 2

Adaptation of gate resistor value to the application conditions

Step 3

Power dissipation

Step 4

Design steps

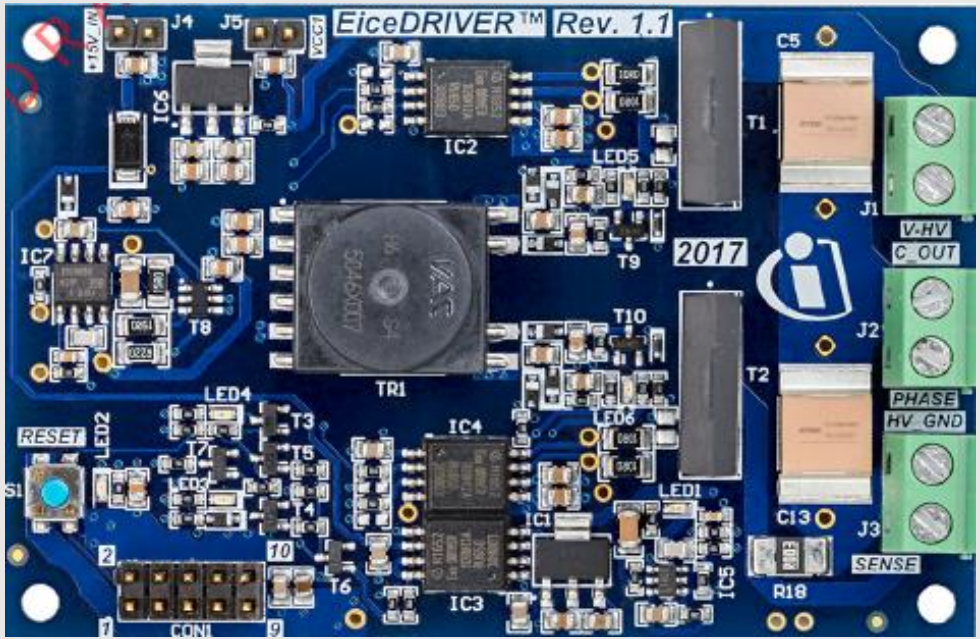
Validate absence of oscillations and parasitic turn-on
Verify thermal behavior of gate driver IC in the application




Step 1	Step 2	Step 3	Step 4
Peak current and gate driver IC selection	Adaptation of gate resistor value to the	Power dissipation	Laboratory validation

Design steps may be fully iterated or partially iterated until the final selection is done

Design example
Eval-1EDC20H12AH-SiC



SiC MOSFET: IMZ120R045M1

Positive gate voltage: V_{VCC2} = 15 V

Negative gate voltage: V_{VEE2} = -2 V

Max. switching frequency: $f_{sw} \leq$ 100 kHz

Max. ambient temperature: $T_a \leq$ 85 °C

Gate driver design step 1
Calculation of peak gate current I_G

Evaluation board **EVAL-1EDC20H12AH-SiC, IMZ120R045M1** CoolSiC™ 1200 V SiC Trench MOSFET

$$I_G = \frac{\Delta V_{GS,datasheet}}{R_{G,datasheet} + R_{G,int}}$$

Table Switching characteristics, T_{vj}=25°C

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Turn-on delay time	$t_{d(on)}$	V_{DD}=800V, I_D=20A,	-		-	ns
Rise time	t_r	V_{GS}=-5V/15V, $R_{G,ext}$=2Ω,	-		-	ns

Table Static characteristics (at T_{vj}=25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Internal gate resistance	$R_{G,int}$	f=1MHz, V_{AC} = 25mV	-	4	-	Ω

Gate driver design step 1
Calculation of peak gate current I_G

Evaluation board **EVAL-1EDC20H12AH-SiC, IMZ120R045M1** CoolSiC™ 1200 V SiC Trench MOSFET

$$I_G = \frac{\Delta V_{GS,datasheet}}{R_{G,datasheet} + R_{G,int}} \Rightarrow \Delta V_{GS,datasheet} = |V_{GS(on)}| + |V_{GS(off)}|$$

Table Switching characteristics, T_{vj}=25°C

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Turn-on delay time	$t_{d(on)}$	V_{DD}=800V, I_D=20A,	-		-	ns
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Calculation of peak gate current I_G

Evaluation board **EVAL-1EDC20H12AH-SiC, IMZ120R045M1** CoolSiC™ 1200 V SiC Trench MOSFET

$$I_G = \frac{\Delta V_{GS,datasheet}}{2\ \Omega \quad + \quad 4\ \Omega} \Rightarrow \Delta V_{GS,datasheet} = |\ 15\ V\ | + |\ \ 5\ V\ |$$

Table	Switching characteristics, T_{vj}=25°C					
Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Turn-on delay time	$t_{d(on)}$	V_{DD}=800V, I_D=20A,	-		-	ns
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Gate driver design step 1
Calculation of peak gate current I_G

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$$I_G = \frac{20\ \text{V}}{2\ \Omega \quad + \quad 4\ \Omega} = 3.33\ \text{A}$$

Table Switching characteristics, T_{vj}=25°C

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Turn-on delay time	$t_{d(on)}$	V_{DD}=800V, I_D=20A,	-		-	ns
Rise time	t_r	V_{GS}=-5V/15V, $R_{G,ext}$=2Ω,	-		-	ns

Table Static characteristics (at T_{vj}=25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Internal gate resistance	$R_{G,int}$	f=1MHz, V_{AC} = 25mV	-	4	-	Ω

Gate driver design step 1
Calculation of peak gate current I_G

Evaluation board **EVAL-1EDC20H12AH-SiC, IMZ120R045M1** CoolSiC™ 1200 V SiC Trench MOSFET

$$I_G = \frac{20\ \text{V}}{2\ \Omega \quad + \quad 4\ \Omega} = 3.33\ \text{A}$$

This calculation does not consider any resistance on the gate driver IC or results in worst-case values for the gate driver IC current capability

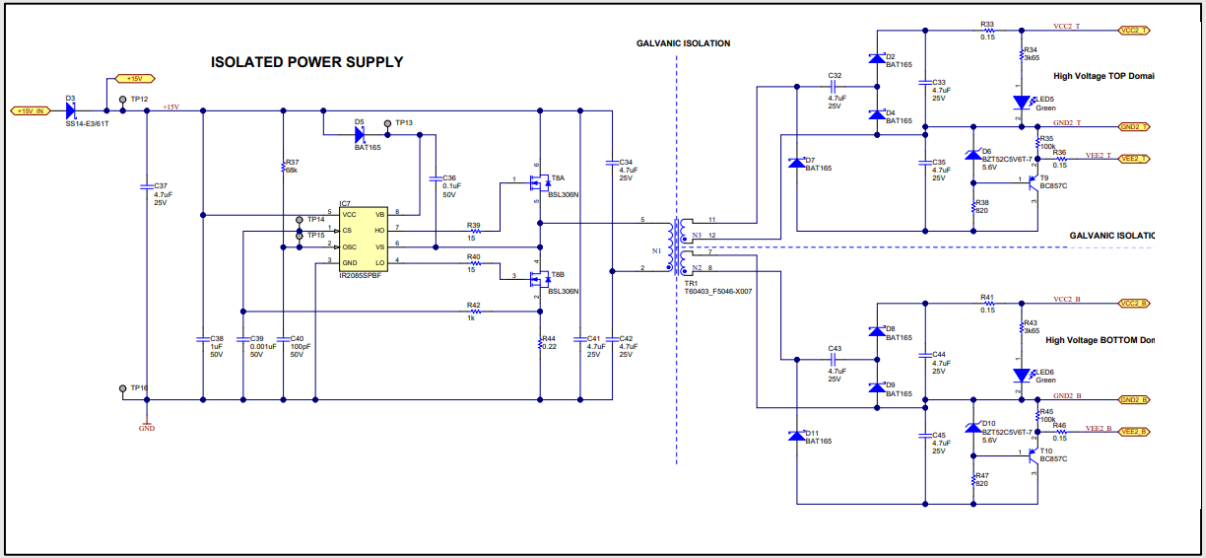
Gate driver design step 1
Gate driver selection

Peak current = 3.33 A

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
High level output peak current (source)	$I_{OUT+,PEAK}$			–	A	[10] IN+ = High, IN– = Low, V_{VCC2} = 15 V
1EDC05I12AH		0.5	1.3			
1EDC20I12AH		2.0	4.0			
1EDC20H12AH		2.0	4.0			
1EDC40I12AH		4.0	7.5			
1EDC60I12AH		6.0	10.0			
1EDC60H12AH		6.0	10.0			
Low level output peak current (sink)	$I_{OUT-,PEAK}$			–	A	[10] IN+ = Low, IN– = Low, V_{VCC2} = 15 V
1EDC05I12AH		0.5	0.9			
1EDC20I12AH		2.0	3.5			
1EDC20H12AH		2.0	3.5			
1EDC40I12AH		4.0	6.8			
1EDC60I12AH		6.0	9.4			
1EDC60H12AH		6.0	9.4			

Gate driver design step 2
Adaptation to application requirements

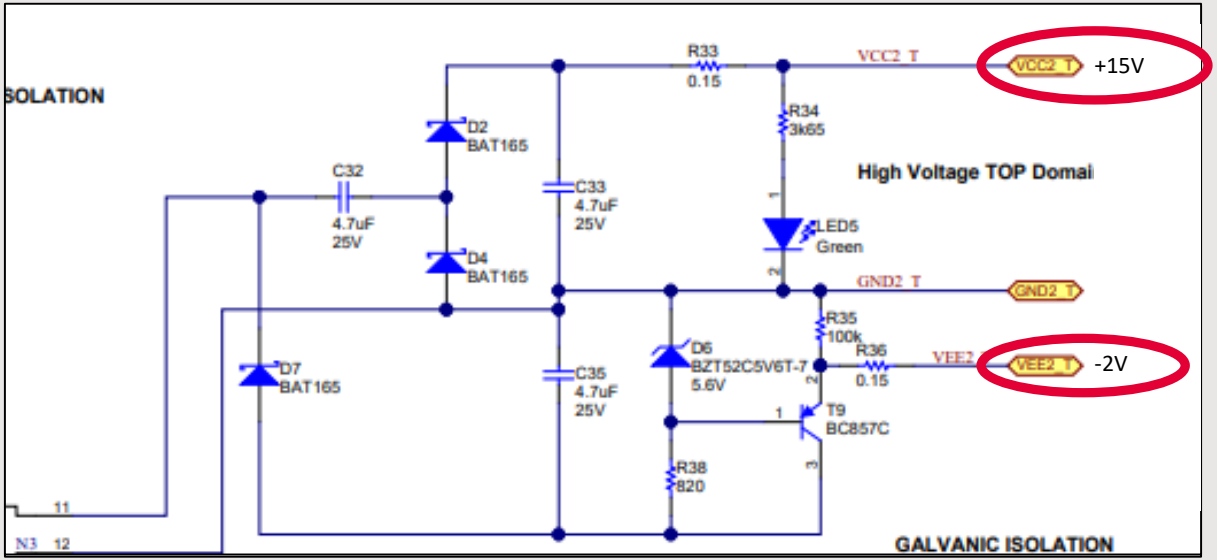
Evaluation board **EVAL-1EDC20H12AH-SiC**



V_{VCC2} = +15 V and V_{VEE2} = -2 V

Gate driver design step 2
Adaptation to application requirements

Evaluation board **EVAL-1EDC20H12AH-SiC**



V_{VCC2} = +15 V and V_{VEE2} = -2 V

Gate driver design step 2
Calculate the external gate resistance R_G

Rearrangement of the equation

$$I_{\mathrm{G,datasheet}} = \frac{\Delta V_{\mathrm{GS,application}}}{R_{\mathrm{G,application}} + R_{\mathrm{G,int}}}$$

Gate driver design step 2
Calculate the external gate resistance R_G

Rearrangement of the equation

$$R_{\mathrm{G,application}} = \frac{\Delta V_{\mathrm{GS,application}}}{I_{\mathrm{G,DS}}} - R_{\mathrm{G,int}}$$

Gate driver design step 2
Calculate the external gate resistance R_G

Rearrangement of the equation

$$R_{\mathrm{G,application}} = \frac{\Delta V_{\mathrm{GS,application}}}{I_{\mathrm{G,DS}}} - R_{\mathrm{G,int}}$$

Table Static characteristics (at T_{vj}=25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Internal gate resistance	$R_{G,int}$	f=1MHz, V_{AC} = 25mV	-	4	-	Ω

Gate driver design step 2
Calculate the external gate resistance R_G

Rearrangement of the equation

$$R_{\mathrm{G,application}} = \frac{17\ \mathrm{V}}{3.33\ \mathrm{A}} - 4\ \Omega = 1.1\ \Omega$$

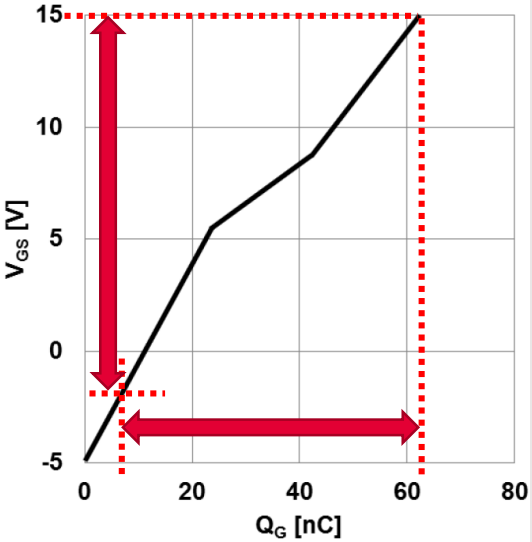
Table Static characteristics (at T_{vj}=25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Internal gate resistance	$R_{G,int}$	f=1MHz, V_{AC} = 25mV	-	4	-	Ω

Gate driver design step 3
Check the power dissipation of the gate driver IC

Power dissipation of the gate driver IC

$$P_{\mathrm{D,Qg}} = Q_{\mathrm{G,application}} \cdot f_{\mathrm{sw}} \cdot \Delta V_{\mathrm{GS,application}}$$



Gate driver design step 3
Check the power dissipation of the gate driver IC

Power dissipation of the gate driver IC

$$P_{D,Qg} = 56\ \text{nC} \cdot 100\ \text{kHz} \cdot 17\ \text{V} = 0{,}095\ \text{W}$$

Curves have to be linearly extrapolated if diagram does not represent the used voltage swing

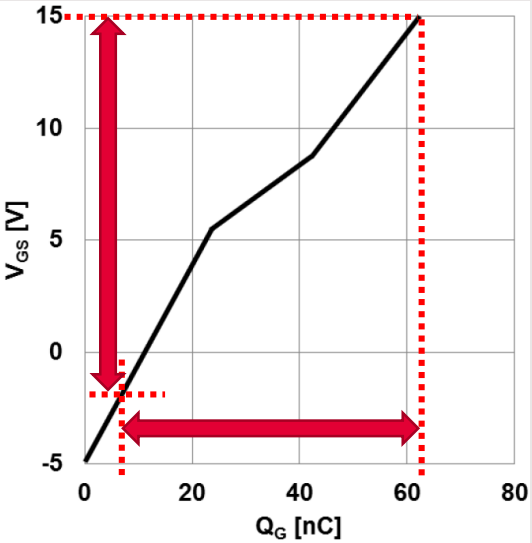
Gate driver design step 3
Check the power dissipation of the gate driver IC

Power dissipation of the gate driver IC

$$P_{\mathrm{D,Qg}} = 56\ \mathrm{nC} \cdot 100\ \mathrm{kHz} \cdot 17\ \mathrm{V} = 0{,}095\ \mathrm{W}$$

$$P_{\mathrm{D,Iq}} = I_{\mathrm{q,2}} \cdot \Delta V_{\mathrm{GS,application}}$$

Quiescent current output chip	I_{Q2}	–	1.2	2.0	mA	V_{VCC2} = 15 V IN+ = High, IN- = Low =>OUT = High



This method often results in **higher dissipated power.**
However this is **on the safe side** and a **simple strategy!**

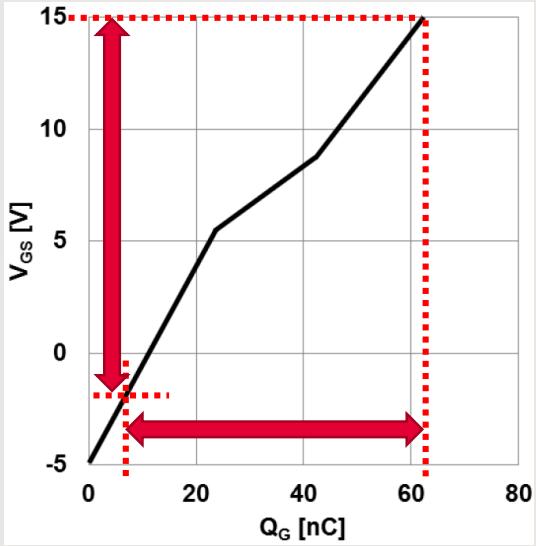
Gate driver design step 3
Check the power dissipation of the gate driver IC

Power dissipation of the gate driver IC

$$P_{\mathrm{D,Qg}} = 56\ \mathrm{nC} \cdot 100\ \mathrm{kHz} \cdot 17\ \mathrm{V} = 0{,}095\ \mathrm{W}$$

$$P_{\mathrm{D,Iq}} = 1.2\ \mathrm{mA} \cdot 17\ \mathrm{V} = 0{,}020\ \mathrm{W}$$

Quiescent current output chip	I_{Q2}	–	1.2	2.0	mA	V_{VCC2} = 15 V IN+ = High, IN- = Low =>OUT = High



Gate driver design step 3
Check the power dissipation of the gate driver IC

Power dissipation of the gate driver IC

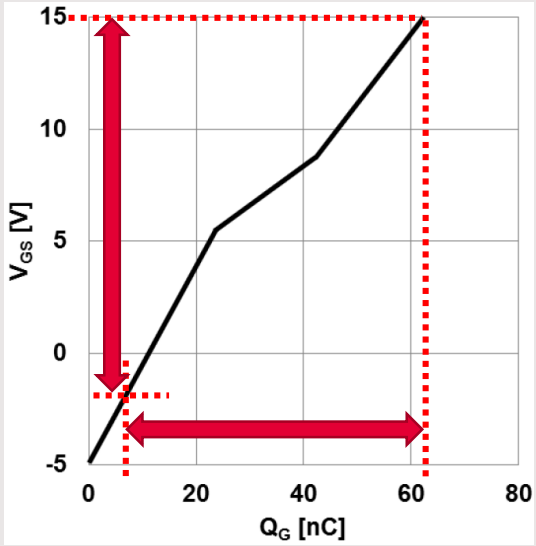
$$P_{D,Qg} = 56\ nC \cdot 100\ kHz \cdot 17\ V = 0{,}095\ W$$

$$P_{D,Iq} = 1.2\ mA \cdot 17\ V = 0{,}020\ W$$

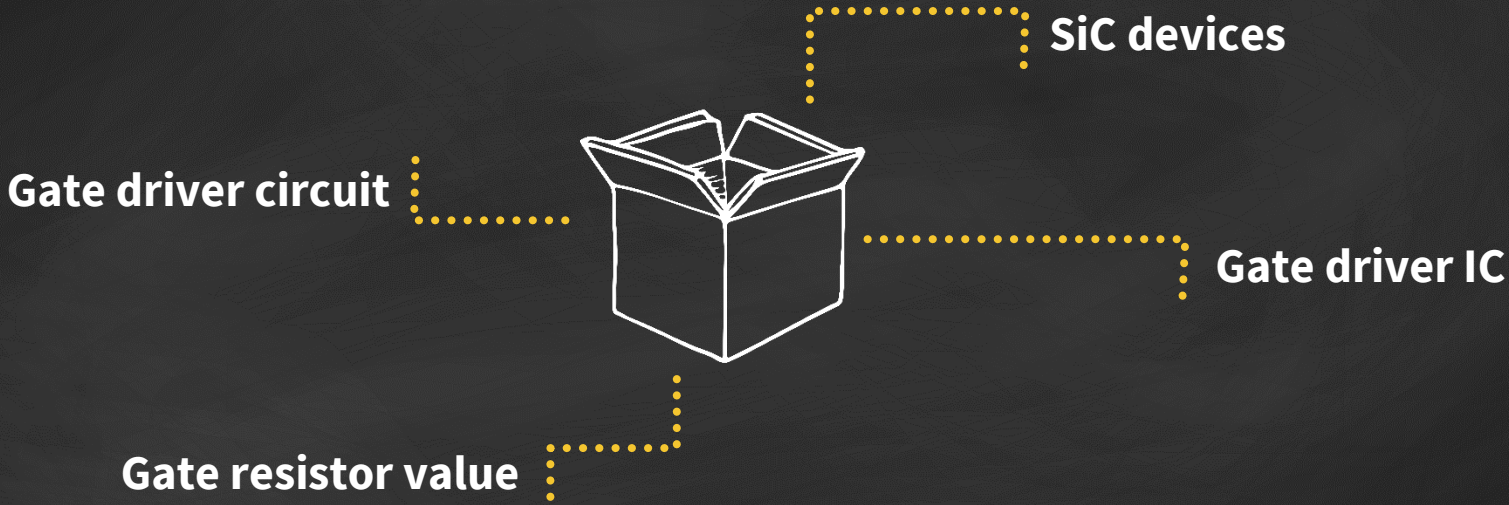
$$P_{D,tot} = 0.095\ W + 0.020\ W = 0{,}105\ W \leq P_{D,OUT}$$

Table 2 Absolute maximum ratings

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Power dissipation (Input side)	$P_{D, IN}$	–	25	mW	2) @T_A = 25°C
Power dissipation (Output side)	$P_{D, OUT}$	–	400	mW	2) @T_A = 25°C



Gate driver design step 4
Target of laboratory verification



Components were selected → design verification in laboratory is required
Lab measurements prove that assumptions and calculations results in safe switching of SiC transistor

Gate driver design step 4
Target of laboratory verification

3 basic tests are recommended

Validations to prove the absence of **parasitic turn-on** triggered by dv_{ds}/dt under worst case conditions

Measurement of **gate driver IC temperature** during steady state operation

Validation of **gate resistor's loading** (R_G)

- Average losses (IR-camera)
- Peak pulse losses (->supplier)

IR camera can help getting the heating of elements (thermocouples are second best)

Peak power of the resistor → calculated and checked against the single pulse rating of the resistor

Gate driver design step 4
Parasitic turn-on robustness

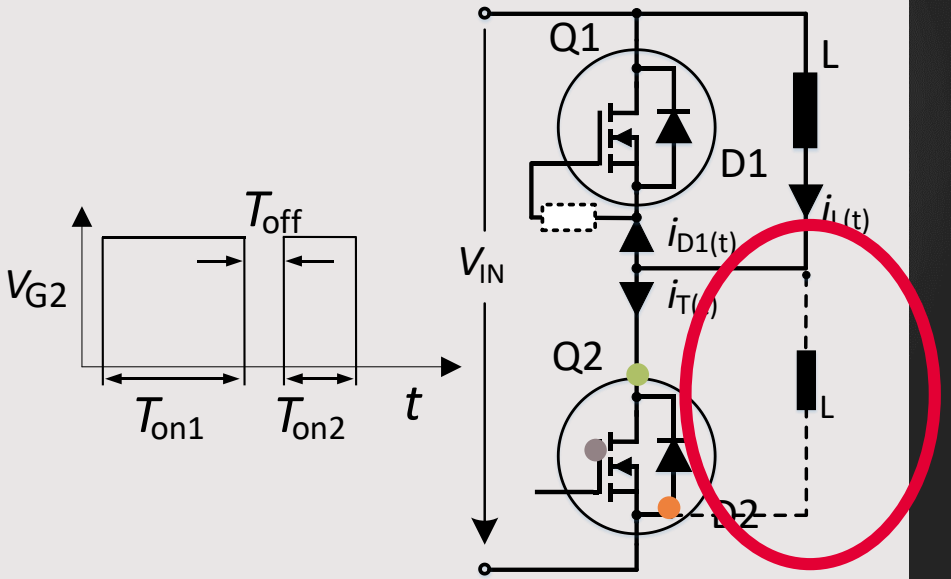
Parasitic turn-on should never occur

Use double pulse test

- High/Low drain current I_D = 0 A / I_{nom}
- High/Low temperature T_j = Min./Max.
- Nominal application gate voltage
- Test both sides of the half-bridge

Measure directly on transistor terminals

- Gate-Source voltage, V_{GS}, across the terminals
- Drain voltage, V_{DS}, across the terminals
- Drain current, I_D



Gate driver design step 4
Examples of parasitic turn-on

Parasitic turn-on can be masked by the diode reverse recovery

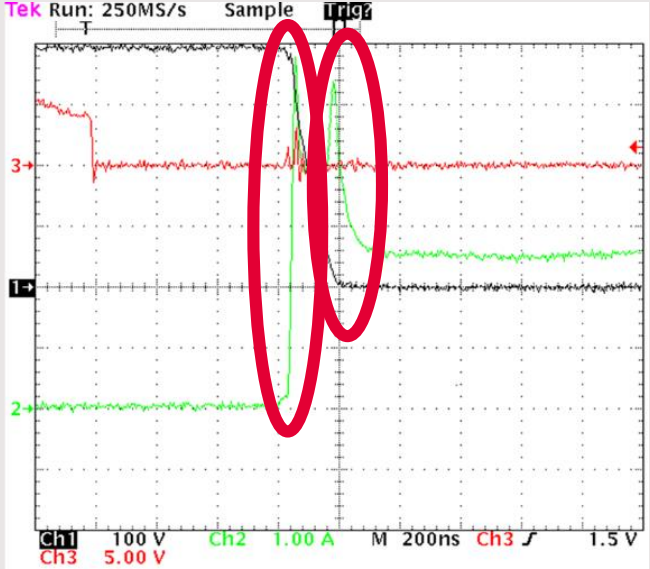


Figure: turn-on of lower side (Q2), measurement at LS emitter shunt
Ch1: Q2 V_{DS} (100 V/div)
Ch2: Q2 I_D (1 A/div)
Ch3: Driver IC $V_{/LIN}$ (5 V/div)
Time: 10 µs/div

First current spike is the reverse recovery of the diode (D1)
Second current spike is the parasitic turn-on in the complimentary switch (Q1)

Gate driver design step 4
Examples of parasitic turn-on

Parasitic turn-on can be masked by capacitive discharge

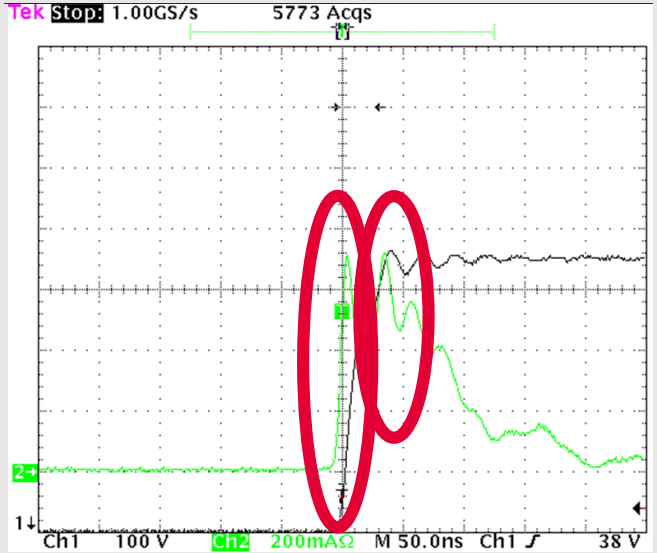


Figure: turn-on of high side (Q1), measurement at LS emitter shunt
Ch1: Q2 V_{DS} (100 V/div)
Ch2: Q2 I_D (200 mA/div)
Ch3: Driver IC $V_{/LIN}$ (5 V/div)
Time: 50 ns/div
T_J: -25°C

First current spike is a capacitive discharge current
Second current spike is the parasitic turn-on of the lower switch (Q2)

Gate driver design step 4
Examples of parasitic turn-on

Parasitic turn-on can be observed also at zero switching current

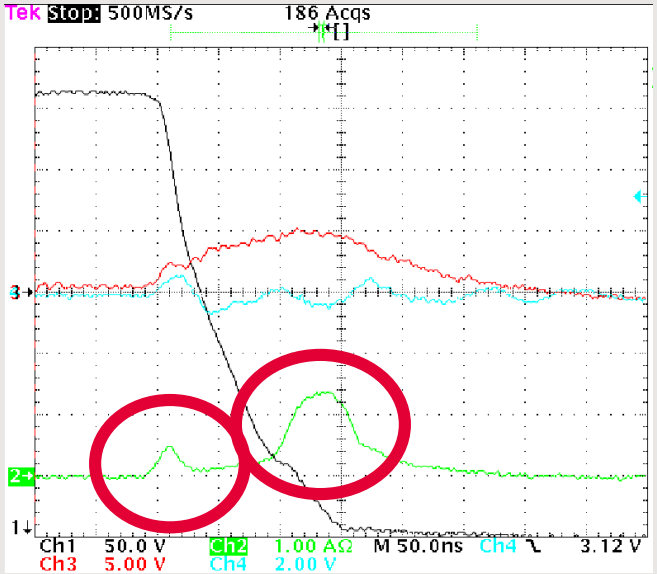
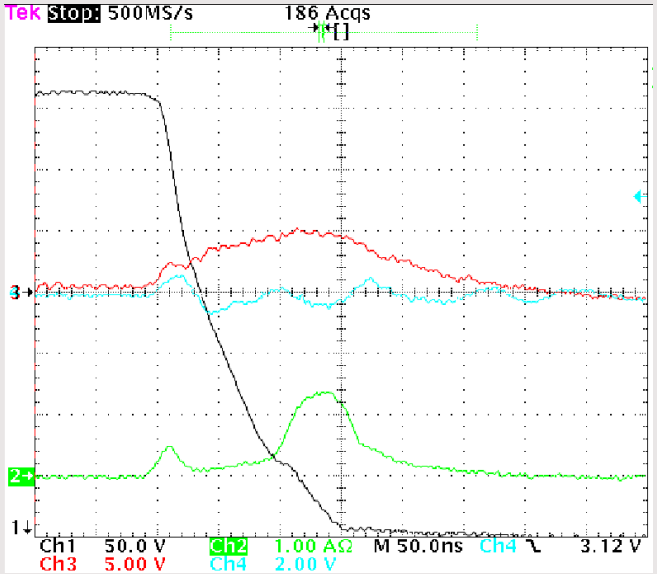


Figure: turn-on of low side (Q2), LS shunt
Ch1: Q2 V_{DS} (50 V/div)
Ch2: Q1 I_D (200 mA/div)
Ch3: Q1 V_{GS} (5 V/div)
Time: 50 ns/div

First current spike is the gate current (Q1)
Second current spike is the parasitic turn-on of the upper switch (Q1) at zero switching current

Gate driver design step 4
Examples of parasitic turn-on

Parasitic turn-on can be observed also at zero switching current



By **increasing gate resistor value**, transistor switching speeds can be slowed down

By choosing a **smaller gate resistor value**, power transistor is switched faster

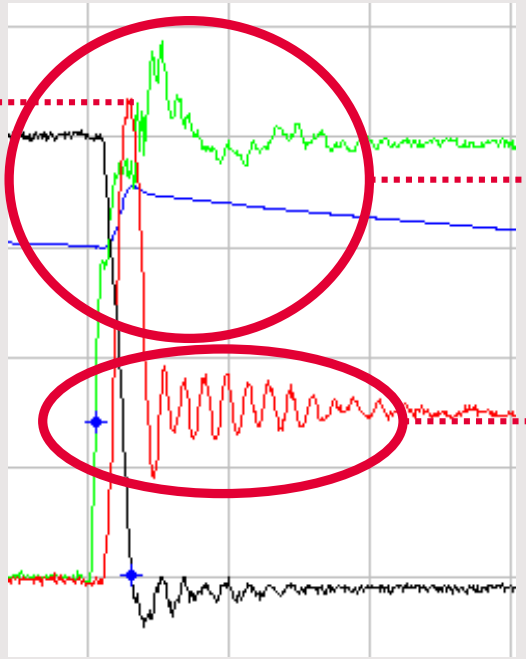
Figure: turn-on of low side (Q2), LS shunt
Ch1: Q2 V_{DS} (50 V/div)
Ch2: Q1 I_D (200 mA/div)
Ch3: Q1 V_{GS} (5 V/div)
Time: 50 ns/div

Gate driver is adjusted and it is confirmed that no parasitic turn-on is taking place!

Gate driver design step 4
Check the switching waveform of gate driver IC + SiC MOSFET

High I_{RRM} = 87 A

Double pulse:
I_D = 30 A
V_{DC} = 800 V
$R_{G,ext}$ = 1 Ω



Oscillations in gate voltage

Oscillations in source current

Black curve: drain-source voltage v_{DS}
Red curve: source current i_S
Green curve: gate-source voltage v_{GS}

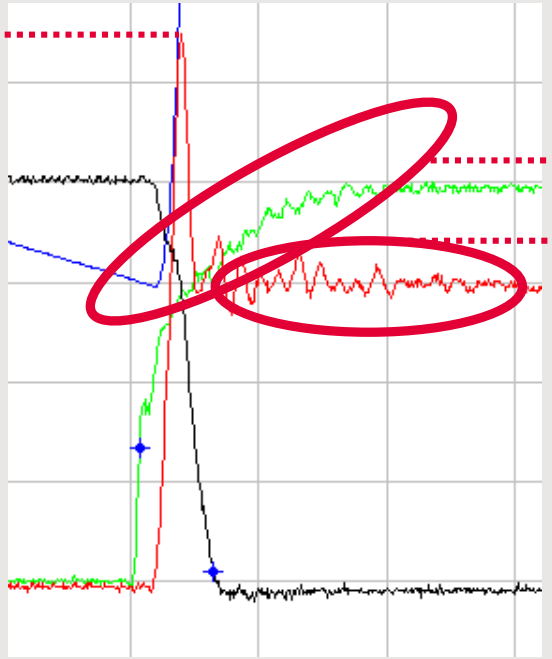
These oscillations are not expected to happen!

A slowdown of switching transient is needed → by increasing gate resistor value

Gate driver design step 4
Check the switching waveform with 10 Ω

Low $I_{RRM} \approx 55$ A

Double pulse:
$I_D = 30$ A
$V_{DC} = 800$ V
$R_{G,ext} = 10$ Ω



Minor oscillations in gate voltage

Acceptable oscillations in emitter current

Black curve: drain-source voltage v_{DS}
Red curve: source current i_S
Green curve: gate-source voltage v_{GS}

Decision of gate resistor → an external gate resistor value of 10 Ω

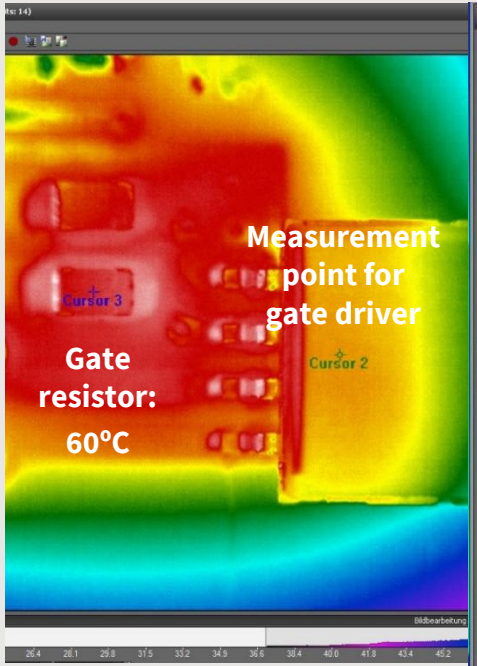
Gate driver design step 4
Check the temperature increase of the gate resistor & driver IC

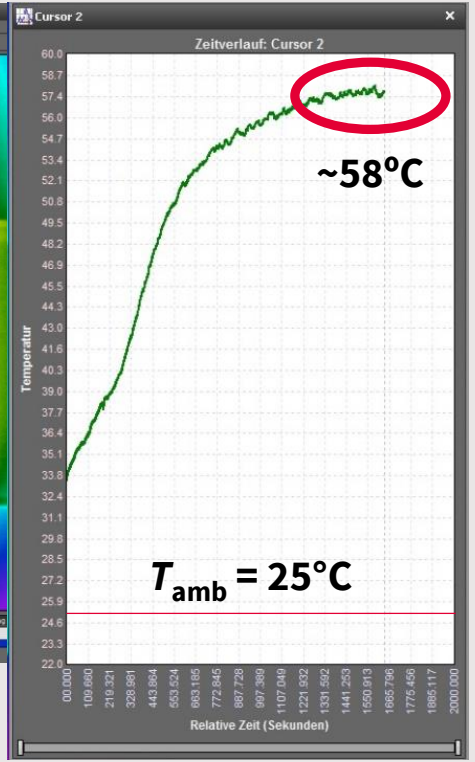
Power dissipation leads to a temperature increase of IC's junction

$$\Delta T_{\mathrm{J,IC}} = P_{\mathrm{D,OUT}} \cdot R_{\mathrm{th(j-a)}} = 0.105\ \mathrm{W} \cdot 165\ \mathrm{°C/W} \approx 17\ \mathrm{°C}$$

58°C – 25°C = 33°C

A dense layout and a close proximity of other heated up components surrounding the gate driver IC can lead to higher temperature than calculated!





Gate driver design step 4
Calculation of peak power stress in gate resistors

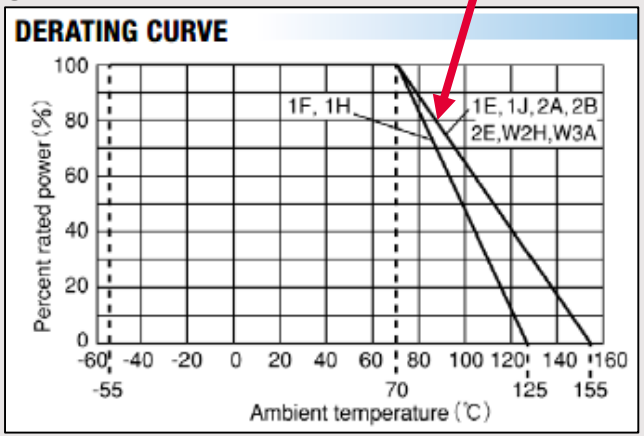
Thermal stress encountered by gate resistor is frequently neglected

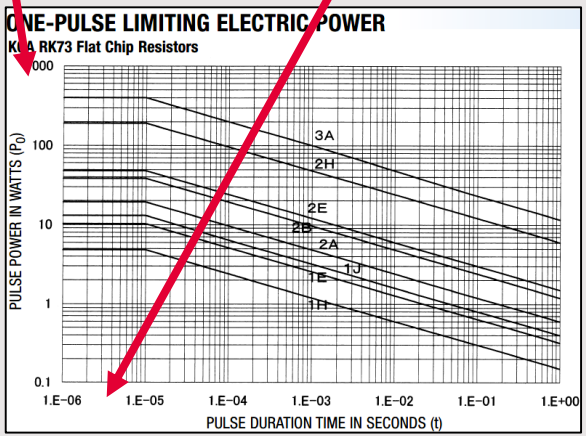
$$P_{\mathrm{Rg,Pk}} = \frac{(V_{\mathrm{VCC2}} - V_{\mathrm{VEE2}})^2}{R_{\mathrm{G}} \cdot 0.8}$$

for a duration of ~R_G*C_{iss} (see AN/datasheet)

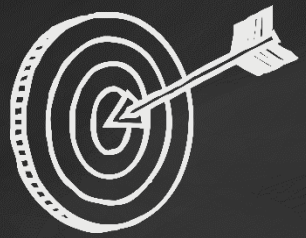
Peak losses include temperature derating of 80%, at 85°C

Datasheet of KOA

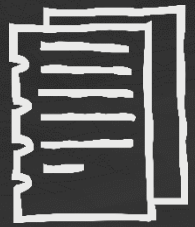




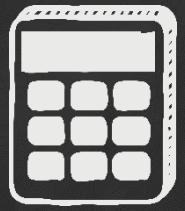
Summary



Gate drivers design has to support the power transistor's characteristics



Power transistor's switching behavior has to be verified experimentally



Power dissipation of the gate driver circuit has to be verified by calculation and temperature measurements

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